DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

COURSE MATERIALS

CS 205 ELECTRONIC CIRCUITS

VISION OF THE INSTITUTION

To mould true citizens who are millennium leaders and catalysts of change through excellence in education.

MISSION OF THE INSTITUTION

NCERC is committed to transform itself into a center of excellence in Learning and Research in Engineering and Frontier Technology and to impart quality education to mould technically competent citizens with moral integrity, social commitment and ethical values.

We intend to facilitate our students to assimilate the latest technological know-how and to imbibe discipline, culture and spiritually, and to mould them in to technological giants, dedicated research scientists and intellectual leaders of the country who can spread the beams of light and happiness among the poor and the underprivileged.

ABOUT DEPARTMENT

- Established in: 2002
- Course offered : B.Tech in Computer Science and Engineering

  M.Tech in Computer Science and Engineering

  M.Tech in Cyber Security
- Approved by AICTE New Delhi and Accredited by NAAC
- Affiliated to the University of Dr. A P J Abdul Kalam Technological University.

DEPARTMENT VISION

Producing Highly Competent, Innovative and Ethical Computer Science and Engineering Professionals to facilitate continuous technological advancement.

DEPARTMENT MISSION

1. To Impart Quality Education by creative Teaching Learning Process
2. To Promote cutting-edge Research and Development Process to solve real world problems with emerging technologies.
3. To Inculcate Entrepreneurship Skills among Students.
4. To cultivate Moral and Ethical Values in their Profession.
5.

PROGRAMME EDUCATIONAL OBJECTIVES

PEO1: Graduates will be able to Work and Contribute in the domains of Computer Science and Engineering through lifelong learning.

PEO2: Graduates will be able to Analyse, design and development of novel Software Packages, Web Services, System Tools and Components as per needs and specifications.

PEO3: Graduates will be able to demonstrate their ability to adapt to a rapidly changing environment by learning and applying new technologies.

PEO4: Graduates will be able to adopt ethical attitudes, exhibit effective communication skills, Teamworkand leadership qualities.

PROGRAM OUTCOMES (POS)

Engineering Graduates will be able to:

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

PROGRAM SPECIFIC OUTCOMES (PSO)

PSO1: Ability to Formulate and Simulate Innovative Ideas to provide software solutions for Real-time Problems and to investigate for its future scope.

PSO2: Ability to learn and apply various methodologies for facilitating development of high quality System Software Tools and Efficient Web Design Models with a focus on performance

optimization.

PSO3: Ability to inculcate the Knowledge for developing Codes and integrating hardware/software products in the domains of Big Data Analytics, Web Applications and Mobile Apps to create innovative career path and for the socially relevant issues.

COURSE OUTCOMES

CO1	To introduce to the students the fundamental concepts of electronic circuits for engineering applications.
CO2	To develop the idea about small signal analysis of CE,CB and CC
CO3	To provide comprehensive idea about High frequency equivalent circuits of BJT, Short circuit current for gain, cutoff frequency, Miller effect
CO4	To equip the students with a sound understanding of fundamental concepts of feedback amplifiers
CO5	To expose to the diversity of operations that oscillators and tuned amplifiers
CO6	To expose to a variety of electronic circuits, Transistor based voltage regulator and MOSFET amplifiers

MAPPING OF COURSE OUTCOMES WITH PROGRAM OUTCOMES

	PO 1	**PO 2**	**PO 3**	**PO 4**	**PO 5**	**PO 6**	**PO 7**	**PO 8**	**PO 9**	**PO 10**	**PO 11**	**PO 12**
CO1	3		3	2	2	2			2			
CO2	3	3	3	2	2	2			2			
CO3	3	3	3	2	2	2			2			
CO4	3	3	3	2	2	2			2			
CO5	3	3	3	2	2	2			2			
CO6	3	3	3	2	2	2			2			

Note: H-Highly correlated=3, M-Medium correlated=2, L-Less correlated=1

PSO MAPPINGS ALSO NEEDS TO INCLUDE

CO'S	PSO1	PSO2	PSO3
C205.1	3	3	2
C205.2	3	3	2
C205.3	3	3	2
C205.4	3	3	2
C205.5	3	3	2
C205.6	3	3	2

SYLLABUS

COURSE CODE	COURSE NAME	L-T-P-C	YEAR OF INTRODUCTION
EC205	ELECTRONIC CIRCUITS	3-1-0-4	2016

Prerequisite: Nil

Course objectives:

- To develop the skill of analysis and design of various analog circuits using discrete electronic devices as per the specifications.

Syllabus:

High pass and low pass RC circuits, Differentiator, Integrator, Analysis of BJT biasing circuits, small signal analysis of transistor configurations using small signal hybrid π model, low frequency and high frequency analysis of BJT amplifiers, Cascade amplifiers, Wide band amplifiers, Feedback amplifiers, Oscillators, Tuned amplifiers, Power amplifiers, Sweep circuits and multivibrators, transistor voltage regulator, DC analysis of MOSFET circuits, small signal equivalent circuit, Small signal analysis of MOSFET amplifier circuits, Analysis of multistage MOSFET amplifiers

Expected outcome:

- At the end of the course, students will be able to analyse and design the different electronic circuits using discrete electronic components.

Text Books:

• Sedra A. S. and K. C. Smith, Microelectronic Circuits, 6/e, Oxford University Press, 2013 • Millman J. and C. Halkias, Integrated Electronics, 2/e, McGraw-Hill, 2010

References:

1. Neamen D., Electronic Circuits - Analysis and Design, 3/e, TMH, 2007
2. Rashid M. H., Microelectronic Circuits - Analysis and Design, Cengage Learning, 2/e, 2011
3. Spencer R. R. and M. S. Ghausi, Introduction to Electronic Circuit Design, Pearson, 2003
4. Razavi B., Fundamentals of Microelectronics, Wiley, 2015

Course Plan			
Module	**Course content (48 hrs)**	**Hours**	**Sem. Exam Marks**
I	RC Circuits: Response of high pass and low pass RC circuits to sine, step, pulse and square wave inputs, Differentiator, Integrator	5	**15**
	BJT biasing circuits: Types, Q point, Bias stability, Stability factors, RC coupled amplifier and effect of various components, Concept of DC and AC load lines, Fixing of operating point , Classification of amplifiers	5	
II	Small signal analysis of CE, CB and CC configurations using small signal hybrid π model (gain, input and output impedance). Small signal analysis of BJT amplifier circuits, Cascade amplifier	7	**15**
FIRST INTERNAL EXAM			
III	High frequency equivalent circuits of BJT, Short circuit current gain, cutoff frequency, Miller effect, Analysis of high frequency response of CE, CB and CC amplifiers	4	**15**
	Wide band amplifier: Broad banding techniques, low frequency and high frequency compensation, Cascode amplifier.	4	
IV	Feedback amplifiers: Effect of positive and negative feedback on gain, frequency response and distortion. Feedback topologies and its effect on input and output impedance, Feedback amplifier circuits in each feedback topologies (no analysis required)	3	**15**
	Oscillators & Tuned Amplifiers: Classification of oscillators, Barkhausen criterion, Analysis of RC phase shift and Wien bridge oscillators, Working of Hartley, Colpitts and Crystal oscillators; Tuned amplifiers, synchronous and stagger tuning	6	
SECOND INTERNAL EXAM			
V	Power amplifiers: Classification, Transformer coupled class A power amplifier, push pull class B and class AB power amplifiers, efficiency and distortion, Transformer-less class B and Class AB power amplifiers, Class C power amplifier (no analysis required)	6	**20**
	Switching Circuits: Simple sweep circuit, Bootstrap sweep circuit, Astable, Bistable, and Monostable multivibrators, Schmitt Trigger	5	
VI	Transistor based voltage regulator: Design and analysis of shunt and series voltage regulator, load and line regulation, Short circuit protection	4	**20**
	MOSFET amplifiers: Biasing of MOSFET amplifier, DC analysis of single stage MOSFET amplifier, small signal equivalent circuit. Small signal voltage and current gain, input and output impedances of CS configuration. MOSFETCascade amplifier	5	

QUESTION BANK

MODULE I				
Q:NO:	**QUESTIONS**	**CO**	**KL**	**PAGE NO:**
1	Describe about **non-linear wave shaping.**	CO1	K2	
2	**Discuss about non-linear network.**	CO1	K3	
3	**List out the applications of voltage comparator.**	CO1	K3	
4	**Explain the operation of positive clamper (Negative peak clamper).**	CO1	K2	
5	**Explain the operation of negative clamper (positive peak clamper).**	CO1	K2	
6	**Explain the working of RC low pass filter, how it can be act as an integrator.**	CO1	K2	
7	**Explain the working of RC high pass filter, how it can be act as an differentiator.**	CO1	K2	
8	**Explain about Sweep circuits? Explain the working of a simple sweep circuit using transistor as a switch with relevant sketches.**	CO1	K2	
9	**Explain the working of Voltage Doubler/Tripler/Quadruppler with help of a neat sketch.**	CO1	K2	
10	**Explain the working of Clamper Circuits with Diagrams.**	CO1	K2	
11	**Explain the working of Clipping Circuits with Diagrams.**	CO1	K2	

	MODULE II			
1	**Expain unregulated power supply is not good ?enough for many applications in electronics?**	CO2	K2	
2	**Discuss about series voltage regulators are called Linear voltage regulators?**	CO2	K2	
3	**List out the limitations of series Voltage regulators**?	CO2	K3	
4	**Explain why BJT is called bipolar device while FETs are called Unipolar device?**	CO2	K4	
5	**Draw the circuit diagram of Zener-voltage regulator and explain how line & Load regulation is achieved in the circuit.**	CO2	K3	
6	**Explain with diagram the fold back current limiting circuit.**	CO2	K2	
7	**Explain how short circuit & overload protection is achieved in series voltage regulators.**	CO2	K2	
8	**Explain with sketches the working of IC 723 as Low & high Voltage regulator.**	CO2	K2	
9	**Draw the block diagram & Explain 3 terminal voltage regulators.**	CO2	K4	
10	**Explain with diagram the functioning of SMPS.**	CO2	K2	
11	**Define pinch –off voltage of a JFET and explain its significance?**	CO2	K1	
12	**Draw the Structural diagram of MOSFET and explain its operation.**	CO2	K2	
13	**Draw the Structural diagram of N- Channel JFET and explain its operation.**	CO2	K2	
	MODULE III			
1	**Define Stability factor & derive the general expression for stability factor.**	CO3	K1	
2	**Discuss about multistage amplifier circuit?**	CO3	K3	
3	**Explain about cascaded amplifiers? Explain the**	CO3	K2	

	effect of cascading on Gain & Bandwidth.			
4	**Draw fixed Biased circuit & derive its Stability factor.**	CO3	K3	
5	Expain about voltage divider bias circuit.Derive the expression for stability factor	CO3	K4	
6	Expain about dc load and ac load line	CO3	K2	
7	Expalin detail about multistage amplifiers	CO3	K2	
8	Draw the neat diagram of common source amplifier with neat diagram	CO3	K3	
9	Expain about effect of negative feed back on amplifier	CO3	K2	
10	Draw the circuit dagram of direct coupled amplifier,Explain its working	CO3	K3	
	MODULE IV			
1	**Draw the circuit & explain the working of Wein bridge oscillator. Also derive its frequency of operation.**	CO4	K3	
2	**Explain the concept involved in crystal oscillator with its characteristics?**	CO4	K2	
3	**Explain Bistable Multivibrator**	CO4	K2	
4	**Explain about collector coupled Astable Multivibrator**	CO4	K2	
5	**Explain emitter coupled Astable Multivibrator**	CO4	K2	
6	**Draw and explain a one-shot circuit.**	CO4	K2	
7	**Discuss the conditions for sustained oscillator or what is Barkhausen criterion?**	CO4	K3	
8	**List out the classifications of Oscillators?**	CO4	K3	

9	**Explain types of feedback oscillators?**	CO4	K2	
10	**List the conditions for oscillation?**	CO4	K2	
11	**Define Piezoelectric effect.**	CO4	K1	
12	**Explain Miller crystal oscillator? Explain its operation.**	CO4	K2	
	MODULE V			
1	**Compare ideal and practical Op-Amp parameters**	CO5	K3	
2	**Explain Slew Rate & what causes slew rate.**	CO5	K2	
3	**Explain the application Op-Amp as Sign Changer & Scale Changer.**	CO5	K3	
4	**Write Notes on Integrator & Differentiator using Op-Amp.**	CO5	K3	
5	**Explain the application Op-Amp as Summing & Difference Amplifier**	CO5	K2	
6	**Draw and explain Schmitt trigger Using Opamp**	CO5	K3	
7	**Draw the circuit diagram of Wien bridge oscillator Using Op amp & Explain its operation.**	CO5	K3	
	MODULE VI			
1	**List-out the Advantages & Disadvantages of Active filters over Passive filters.**	CO6	K3	
2	**Explain about Butterworth filters? Explain its Ist order LP & HP filters.**	CO6	K2	
3	**Draw and explain 2nd order Butterworth LPF & HPF**	CO6	K2	
4	**Explain with a diagram the principle of working of Sample & Hold Circuit.**	CO6	K2	
5	**List out the specifications of Digital to Analog Converters**	CO6	K3	

6	**Explain the working of Dual slope ADC with the help of a Diagram**	CO6	K2	
7	**Explain the working of SAR & Flash type ADCs with the help of a Diagram**	CO6	K2	
9	**Draw the Functional block Diagram of 555 Timer IC and Explain its operation as Astable-Multi vibrator.**	CO6	K3	
10	**Draw the Diagram of Monostable Multi-vibrator using 555 IC and explain its operation**	CO6	K3	
11	**Design a Butterworth LPF having Cutoff frequency of 2 KHz and pass band gain of 2.5**	CO6	K5	
12	**Design a second order LPF at cutoff frequency 1KHz**	CO6	K5	
13	**Determine the resolution of a). 6 Bit DAC b). 12 Bit DAC in terms of percentage**	CO6	K5	
14	**Design a 4 bit weighted Resistor DAC whose full scale output voltage is -5V.logic levels are 1= +5V; 0= -5V.What is the output voltage when input voltage is 1101**	CO6	K5	
15	**An 8 bit DAC produce Vout = 0.05V for a Digital input of 00000001.Find full scale output. What is its resolution. What is output for an input of 00101010**	CO6	K5	

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MODULE 1

EC 205

BJT-AMPLIFIERS

BIASING OF TRANSISTOR

Biasing in general means to establish predetermined voltages and currents at specific points of a circuit, so that the circuit components will operate normally. For transistors, biasing means to set the proper voltage and current of the transistor base, thus setting the operating point, also known as quiescence point (*Q*). For now, you need to know that this point will determine how the transistor will operate (amplifier or switch). A correctly placed *Q* offers maximum amplification without signal distortion or clipping.

Only the fixing of suitable operating point is not sufficient ,it must also be ensure that it should remain where it was fixed. There are two reasons for operating point to shift.

1. The transistor parameters are temperature dependent.
2. The parameters such as β changes from unit to unit.

Flow of current in the collector circuit produces heat at the collector circuit. This increases the temperature and more minority carriers are generated in the base collector junction .Since more bonds are broken and the resulting leakage current *Ico (Icbo)* increases.

$Ic = \beta\, Ib + (\beta+1) Icbo$

But $(\beta+1) Icbo = Iceo$

$Ic = \beta Ib + Iceo$

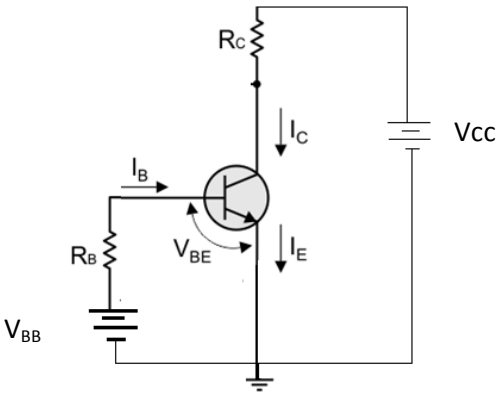
The increase in *Icbo* will cause *Iceo* to increase which in tern increase the collector current Ic. This further rises the temperature at collector base junction and the whole cycle repeats again. Such a cumulative increase in Ic will ultimately shift the operating point into saturation region. The excess heat produces at the junction even burn the transistor.Scch a situation is described by the term *Thermal run away* .

OPERATING POINT & DC LOAD LINE ANALYSIS

For proper operation of the transistor ,whether the signal(i.e. ac input)is present or not ,a fixed level of currents and voltages are required. These values of currents and voltages define a point at which the transistor operates. This point is called'" *Operating point or Quiscent point"* .Since the level of currents and voltages are fixed, then the operating point is also fixed.

Let us consider a transistor circuit as shown in figure. In this case the transistor is biased with two dc supplies ,namely Vcc and VBB to provide fixed amount of voltage and current to emitter and collector terminals. VBB used to make emitter base junction properly forward biased and Vcc makes the base collector junction becomes reverse biased.

First of all ,adjust VBB to produce a fixed base current, then the corresponding value of collector current will be Ic= β I_B .Adjust Vcc makes output junction reverse biased and Vce can be calculated as follows.



Apply KVL to the output circuit

$Vcc = Vce + IcRc$

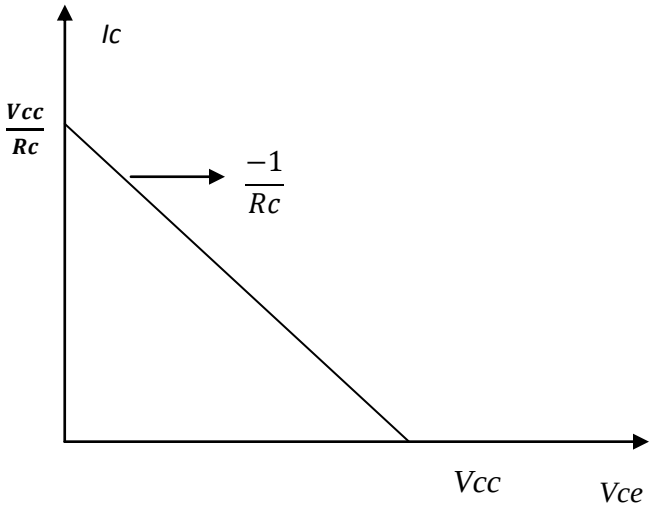
$Vce = Vcc - IcRc$

ie. $Ic = \frac{(Vcc - Vce)}{Rc}$: $Ic = \left(\frac{-1}{Rc}\right) Vce + \frac{Vcc}{Rc}$

$Ic = \frac{Vcc}{Rc}$ for Vce=0

Ic=0; for Vce= Vcc

DC load line



The DC load line can be defind as a line on the output characteristics of a transistor which gives the values of Ic & Vce corresponding to Zero signal condition.

The Dc load line gives the following informations;

1. The load line intersects the horizondal axis at a point marked Vcc which is called transistor "Cutoff point". At this point the values of IB & Ic are zero.
2. The load line intersects the vertical axis at point marked as Ic is called "Saturation point" . At tis point Ic is maximum, and Vce is zero.

STABILITY FACTOR

The extent to which the collector current *Ic* is stabilized with varying *Ico* is measured by stability factor "S".It is defind as the rate of change of collector current w.r.t. *Ico* keeping both IB and current gain β as constant.

$$S = \frac{dIc}{dIco} = \frac{\Delta Ic}{\Delta Ico}$$

When the transistor is biased in the active region of its characteristics ,the collector current Ic is related to base current Ib by following expression

IC=βIB+(β+1)Ico

Differentiating w.r.t Ic considering β as constant we get,

$$=\beta \frac{dIB}{dIc} + (\beta+1)\frac{dIco}{dIc}$$

$$= \beta \frac{dIB}{dIc} + \frac{(\beta+1)}{S}$$

$$S = \frac{(\beta+1)}{1-\beta\frac{dIB}{dIc}}$$

A higher value of stability factor indicates lower stability and low value indicates good stability. ***Unity*** is the lowest value of stability factor. Since $S = \frac{dIc}{dIco}$ it may be noted that as the value of stability factor closes to unity the variation of collector current with temperature will be less. There fore there will be less variation in ***Q point.***

Stability factors S′ and S″

The stability factor S′ is defined as the rate of change of Ic with VBE keeping Ico and β constant.

$$S' = \frac{dIc}{dVBE} = \frac{\Delta Ic}{\Delta VBE}$$

Stability factor S'' is defined as the rate of change of Ic w.r.to β,Keeping Ico and Vbe constant.

$$S'' = \frac{dIc}{d\beta} = \frac{\Delta Ic}{\Delta \beta}$$

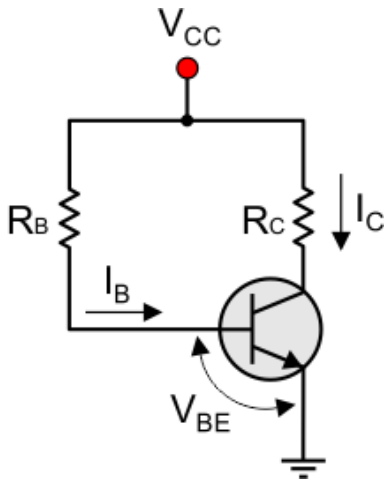
TYPES OF BJT BIASING

The different methods for providing bias for a transistor is as follows:

1) Base resistor method or Fixed Bias
2) Emitter feedback bias (Fixed bias with emitter resistor)
3) Collector to Base Bias
4) Voltage divider Bias or Self bias

Base resistor method or Fixed bias

This is the most rarely used biasing method with transistor amplifiers, but it is widely used when the transistor operates as a switch.



The base current I_B is controlled by the base resistor R_B. From the second law of Kirchhoff, we have:

Vcc=IbRb+Vbe ----------(1)

Or Ib=$IB = \frac{(Vcc - VBE)}{RB}$ or Rb= $\frac{(Vcc - VBE)}{IB}$ ----------(2)

We know Ic/Ib= β and Vbe<< Vcc

Therefore Ib = Vcc/Rb

Or $Rb = \frac{Vcc}{Ib} = \frac{\beta Vcc}{Ic}$ ----------(3)

In this case ,if Vcc,β are fixed values then Ic is also fixed for a given transistor due to which Rb is also a fixed value.So this method is called as *Fixed Bias Method.*

Stability factor S

The stability factor S can be defined as the rate of change of collector current w.r.t reverse saturation current assume β and Vbe constant.

$S = \frac{dIc}{dIco} = \frac{(\beta+1)}{1-\beta\frac{dIB}{dIc}}$

To obtain S Differentiate equation (2) w.r.t Ic

$\frac{dIB}{dIc}$ = 0 because Vcc,Vbe & Rb are constants.

S = (1+β) ----------(4)

If β = 100 then S=101 , it clearly shows that Ic is more dependent on Ico and Tempereture.It causes poor stabilization. These are the dis advantages of this method.

Stability factor S′

$\boldsymbol{S' = \frac{dIc}{dVBE}}$ when β and Vbe are constants.

$= \frac{d}{dVbe}\beta[\frac{Vcc-Vbe}{Rb}]$

$S' = \frac{-\beta}{Rb}$

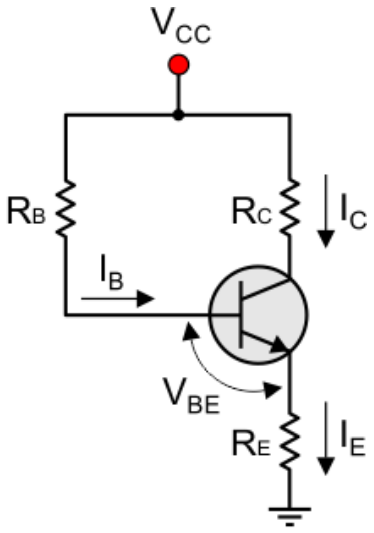
Stability factor S″

$S'' = \frac{dIc}{d\beta}$

$= \frac{d}{d\beta}\beta[\frac{Vcc-Vbe}{Rb}]$

$S'' = \frac{Vcc-Vbe}{Rb}$

Emitter feedback bias (Fixed bias with emitter resistor)



Applying KVL at input

Vcc- IbRb- Vbe-IeRe=0;

Vcc- IbRb- Vbe-(1+β)IbRe=0;

Ib(Rb+(1+β)Re= Vcc-Vbe

$$Ib = \frac{Vcc - Vbe}{Rb + (1+\beta)Re}$$

$$Ic = \beta \left[\frac{Vcc - Vbe}{Rb + (1+\beta)Re}\right]$$ here $(1+\beta) \approx \beta$

$$\therefore Ic \cong \frac{Vcc - Vbe}{Re}$$ *ie*. Ic donot depend on β

Stability factor S

$$\frac{dIB}{dIc} = 0$$

∴ S = (1+β)

Stability factor S'

$$S' = \frac{dIc}{dVBE} = \frac{d}{dVBE}\beta\left[\frac{Vcc - Vbe}{Rb + (1+\beta)Re}\right]$$

$$S' = \frac{-\beta}{Rb + (1+\beta)Re}$$

Stability factor S''

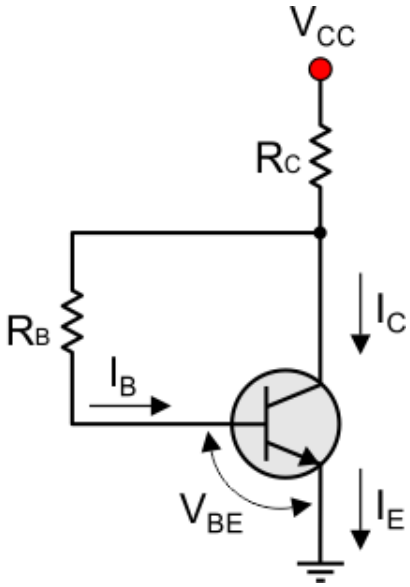
$$S'' = \frac{dIc}{d\beta} = \frac{d}{d\beta}\beta\left[\frac{Vcc - Vbe}{Rb + (1+\beta)Re}\right]$$

$$S'' = \frac{[Rb + (1+\beta)Re][Vcc - Vbe] - (Vcc\,\beta - Vbe\,\beta)Re}{(Rb + (1+\beta)Re)2}$$

$$S'' = \frac{[Vcc - Vbe][Rb + Re + \beta Re - \beta Re]}{(Rb + (1+\beta)Re)2}$$

$$S'' = \frac{[Vcc - Vbe][Rb + Re]}{(Rb + (1+\beta)Re)2}$$

Collector feedback bias (Collector to base bias)



Circuit Analysis

The required Rb needed to give the zero signal current Ic is calculated as follows.

Apply KVL at i/p circuit:

Vcc- (Ib+Ic)Rc-IbRb-Vbe = 0

Ib(Rc+Rb)=Vcc-Vbe-IcRc

$Ib = \frac{Vcc - Vbe - IcRc}{(Rc+Rb)}$ ---------- (1)

Stability factor S

$S = \frac{dIc}{dIco} = \frac{(\beta+1)}{1-\beta\frac{dIB}{dIc}}$

Differentiate eqn.(1) w.r.t Ic we get:

$$\frac{dIb}{dIc} = 0 - \frac{Rc}{Rc+Rb}$$

$$\frac{dIb}{dIc} = \frac{Rc}{Rc+Rb}$$

$\therefore S = \frac{(\beta+1)}{1-\beta\frac{Rc}{Rc+Rb}}$

Stability factor S'

$\mathbf{S'} = \frac{dIc}{dVBE}$ when β and Vbe are constants.

From eqn.(1) $Ib = \frac{Vcc - Vbe - IcRc}{(Rc+Rb)}$

Or $\frac{Ic}{\beta} = \frac{Vcc - Vbe - IcRc}{(Rc+Rb)}$ or $\frac{Ic}{\beta} + \frac{IcRc}{(Rc+Rb)} = \frac{Vcc - Vbe}{(Rc+Rb)}$

Or $Ic[Rc+Rb+\beta Rc] = (Vcc - Vbe)\beta$

Or $Ic = \frac{\beta(Vcc - Vbe)}{Rb + Rc(1+\beta)}$

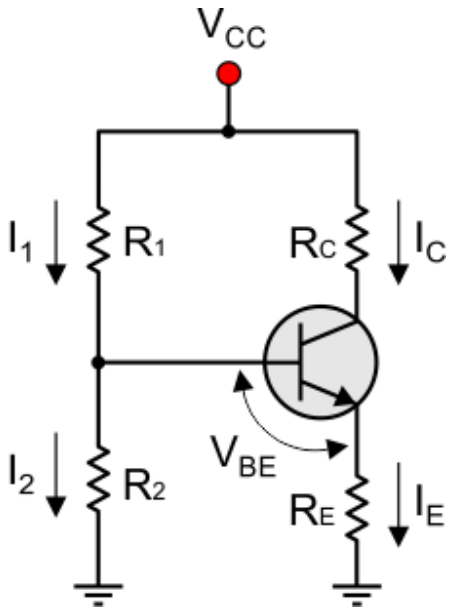
$$\therefore \quad S' = \frac{dIc}{dVBE} = \frac{-\beta}{Rb+Rc(1+\beta)}$$

$$S' \cong \frac{-1}{Rc}$$

Stability factor S''

$$S'' = \frac{dIc}{d\beta} = \frac{d}{d\beta}\beta\left[\frac{Vcc-Vbe}{Rb+(1+\beta)Rc}\right] = \frac{(Vcc-Vbe)(Rc+Rb)}{[Rb+(1+\beta)Rc]2}.$$

Voltage Divider Biasing

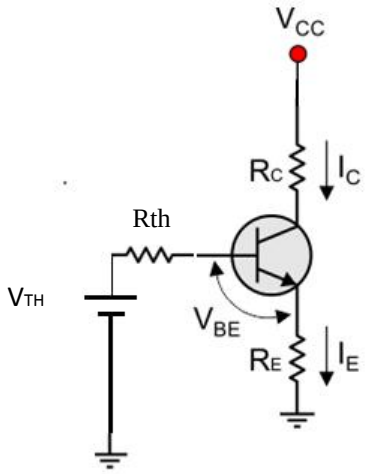


In this method two resistors R1 and R2 acts as potential devider and are connected across supply voltage Vcc to provide Biasing.

The improvement in operating point stability may be explained as follows :

Let there be a rise in temperature , this causes a rise in Ico,ie rise in Ic.Now the current in Re increases,as a result the voltage drop in Re increases and consequently the base current decreases.

Thevanian Eqivqlent circuit



$$Vth = Vcc\frac{R2}{(R1+R2)}$$

$$Rth = R1\text{II R2}$$

$$=\frac{R1R2}{R1+R2}$$

Applying KVL in the i/p side :

Vth-Ib.Rth-Vbe-Ie.Re = 0 : Vth-Ib.Rth-Vbe-(β+1)Ib.Re = 0.

Ib[Rth+((β+1).Re] = Vth-Vbe

Ib = $\frac{\text{Vth} - \text{Vbe}}{\text{Rth} + ((\beta+1).\text{Re}}$; Ic = β. $\frac{\text{Vth} - \text{Vbe}}{\text{Rth} + ((\beta+1).\text{Re}}$

(β+1)≅ β and Re >> $\frac{Rth}{\beta}$

∴ $Ic = \frac{\beta(Vth-Vbe)}{\beta(\frac{Rth}{\beta}+Re)}$; $Ic = \frac{Vth-Vbe}{Re}$ ----------(1)

Applying KVL at o/p side :

$Vcc - IcRc - Vce - IcRe = 0$: $Ie \cong Ic$ $[since\ Ib\ is\ very\ small]$

$Vcc - IcRc - Vce - IcRe = 0$

$Vce = Vcc - Ic(Rc + Re)$ ----------(2)

Since both Eqns are independent of β the ***Voltage devider biasing*** circuit is most commenly used.

Stability factor S

S = $\frac{dIc}{dIco} = \frac{(\beta+1)}{1-\beta\frac{dIB}{dIc}}$

KVL at i/p ; $Vth - IbRth - Vbe - IeRe = 0$

$$Vth - IbRth - Vbe - (Ic + Ib)Re = 0$$

$$Ib[Rth + Re] = Vth - Vbe - IcRe$$

$$Ib = \frac{Vth - Vbe - IcRe}{Re + Rth}$$

$$\frac{dIb}{dIc} = \frac{-Re}{Re+Rth}$$

$$\therefore S = \frac{(\beta+1)}{1+\beta\frac{Re}{Re+Rth}} \quad ; \quad (\beta+1) \approx \beta$$

$$= \frac{\beta}{1+\beta\frac{Re}{Re+Rth}} = = \frac{1}{\frac{1}{\beta}+\frac{Re}{Re+Rth}}$$

$$S = \frac{Re+Rth}{Re}$$

Stability factor S'

$$S' = \frac{\boldsymbol{dIc}}{\boldsymbol{dVBE}} = \frac{\boldsymbol{d}}{\boldsymbol{dVbe}}\ \boldsymbol{\beta}\left[\frac{Vth-Vbe}{\boldsymbol{Rth}+(\boldsymbol{\beta}+\boldsymbol{1})\boldsymbol{Re}}\right]$$

$$= \frac{-\boldsymbol{\beta}}{\boldsymbol{Rth}+(\boldsymbol{\beta}+\boldsymbol{1})\boldsymbol{Re}} \quad ; \quad (\beta+1) \approx \beta$$

$$= \frac{-\boldsymbol{\beta}}{\boldsymbol{Rth}+\boldsymbol{\beta}\boldsymbol{Re}}$$

$$\boldsymbol{S'} = \frac{-1}{Re}$$

Stability factor S″

$$S'' = \frac{dIc}{d\beta} = \frac{d}{d\beta}\,\beta\left[\frac{Vth-Vbe}{Rth+(\beta+1)Re}\right]$$

$$= \frac{[Rth+(\beta+1)Re][Vth-Vbe]-\beta[Vth-Vbe]Re}{[Rth+(\beta+1)Re]2}$$

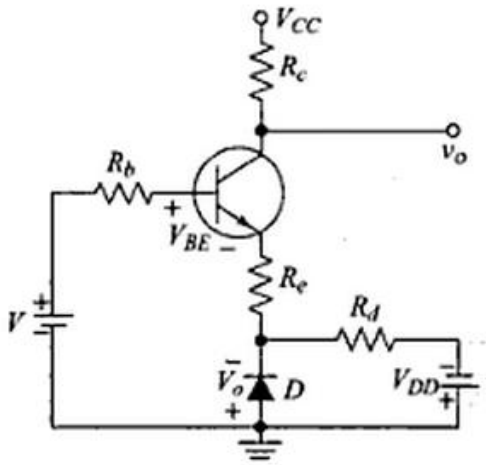
$$= \frac{[Vth-Vbe][Rth+\beta Re+Re-\beta Re]}{[Rth+(\beta+1)Re]2}$$

$$S'' = \frac{[Vth-Vbe][Re+Rth]}{[Rth+(\beta+1)Re]2}$$

BIAS COMPENSATION

Diode compensation for *Vbe*

The diode is kept in forward direction by the source Vd and resistance Rd. If the diode is Of the same material & type as that of the transistor ,then the voltage Vo across the diode will have the same temperature coefficient [-2.5 mV/1^{0}C] as the Base to emitter voltage Vbe .



KVL at I/P side ;

$$Ic = \beta Ib + (\beta+1)Ico$$

$$= \beta\left[\frac{V-(Vbe-Vo)-IcRe}{Re+Rb}\right] + (\beta+1)Ico$$

$$= \frac{\beta[V-(Vbe-Vo)] + ((\beta+1)(Re+Rb)Ico}{(\beta+1)Re+Rb}$$

$$Ic = \frac{\beta[V-(Vbe-Vo)-IcRe]}{Re+Rb} + (\beta+1)Ico$$

$$= \frac{\beta[V-(Vbe-Vo)-IcRe}{Re+Rb} + ((\beta+1)Ico$$

$$Ic\left[1+\frac{\beta Re}{Re+Rb}\right]=\beta\left[\frac{V-(Vbe-Vo)}{Re+Rb}\right]+(\beta+1)Ico$$

$$ie.\ \ Ic=\frac{\beta\{V-(Vbe-Vo)\}+(\beta+1)(Re+Rb)Ico}{(\beta+1)Re+Rb}$$

It is clear from the eqn. that *Ic* is insensitive to variations in *Vbe* due to temperature changes.

DIODE COMPENSATION FOR I_{CO}

For Germanium transistors changes in Ico with temperature plays an important role in collector current stability.The diode compensation technique used in fig. offers stabilization against variations with *Ico.*

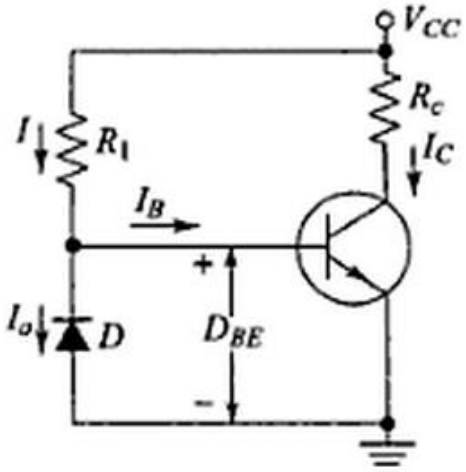


Fig shows the diode of the same meterial as that of transistor for providing the bias compensation.The diode is reverse biased by base emitter junction voltage.It allows reverse saturation voltage or leakage current Ico to flow through it when temperature increases.The reverse saturation current through the transistor also increases, this inturn increases the leakage current through the diode.this will redusethe base current by keeping I constant.This action is required to keep constant values of collector current.

$$Ib=(I-Io)$$

Ic=βIb+(β+1)Ico

$$Ic=\beta(I-Io)\ +(\beta+1)Ico$$

$$Ic=\beta I-\beta Io+\beta Ico+Ico$$

$$Ic=\beta I-\beta Io+\beta Ico$$

BJT Small-Signal Equivalent Circuit Models

In order to develop these Bjt small signal models, there are two small-signal resistances that we must first determine. These are

1. $r\pi$: the small-signal, active mode input resistance between the base and emitter, as "seen looking into the base."
2. r_e : the small-signal, active mode output resistance between the base and emitter, as "seen looking into the emitter."

Determine $r\pi$

Assuming the transistor in this circuit operating in the active region then;

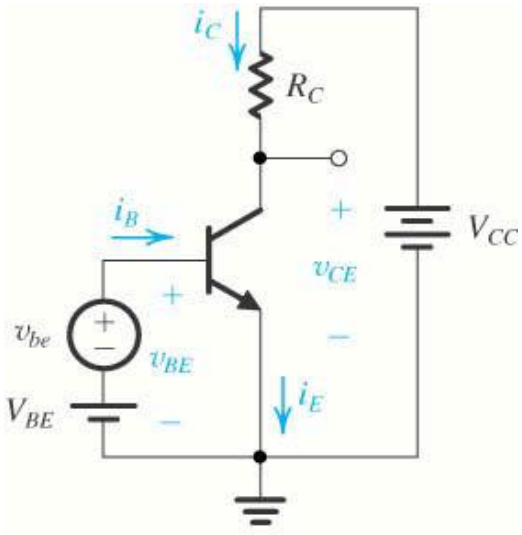
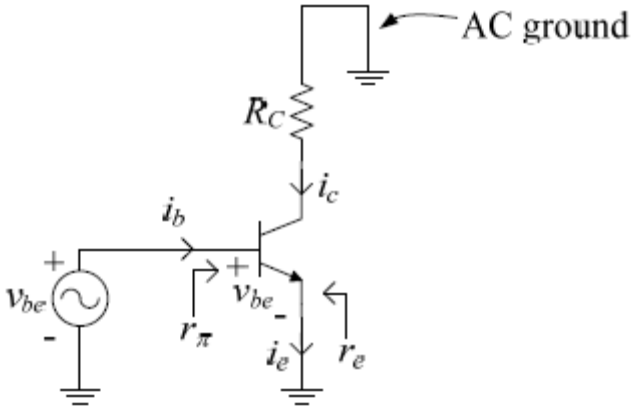


Fig. 1

$i_B = \frac{ic}{\beta} = \frac{1}{\beta}\left[Ic + \frac{Ic}{Vt}Vbe\right]$ ----------(1)

$ib = \frac{Ic}{\beta Vt}Vbe = \frac{gm}{\beta}Vbe$ ---------- (2)

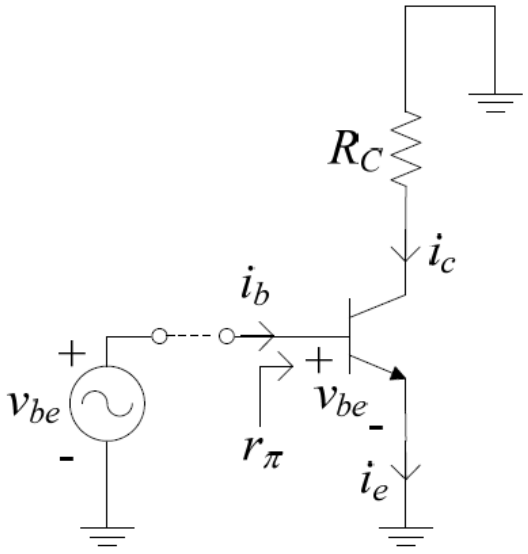
The Ac equivalent circuit of Fig.1 is



Notice the *AC ground* in this circuit.It is *Extreamly important* concept.Since the voltage at this terminal is held at constant voltage Vcc, there is no time variation of voltage.Consequently ,we can set this terminal to be an "AC ground "in small-signal circuit.

For AC Ground we kill the DC source at that terminal:short circuit voltage sourcer and open circuit current sources.

From small signal equivalent curcuit above,



We see that $r_\pi = \frac{Vbe}{ib}$ ----------(3)

Hence using Eqn.2 in 3

$$r_\pi = \frac{\beta}{gm} \quad (\Omega) \qquad \text{----------(4)}$$

This r_π is the small-signal, active mode input resistance between the base and emitter, as "seen looking into the base.

Determine r_e

We will determine r_e following the same procedure for r_π ,but beginning with;

$$i_E = \frac{ic}{\alpha} = \frac{Ic}{\alpha VT} \text{ ----------(5)}$$

AC Component i_E in eqn 5 is ; $ie = \frac{ic}{\alpha} = \frac{Ic}{\alpha VT} Vbe$------(6)

Or with $I_E = \frac{Ic}{\alpha}$; $ie = \frac{IE}{VT} Vbe$ ----------(7)

Mathematically it is stated as $r_e \equiv \frac{Ve}{-ie}$----------(8)

Assuming an ideal voltage source then $Ve = -Vbe$

$$r_e \equiv \frac{Vbe}{ie} \text{ ----------(9)}$$

Using (7) in this equation we find : $r_e = V_T/I_E$ -------(10)

We know $g_m = Ic/V_T = \alpha I_E/V_T$: $V_T/I_E = \alpha/g_m$

There for using this last result in (10) gives

$r_e = \alpha/g_m$

$$\boldsymbol{r_e \cong 1/g_m} \qquad \textbf{----------(11)}$$

This is the BJT active mode small-signal, output resistance between the base and emitter, as "seen looking into the emitter."

It can be shown that

$$r_{\pi} = (\beta+1)\, r_e \ [\Omega] \quad \text{----------(12)}$$

BJT SMALL SIGNAL EQUIVQLENT CIRCUITS

HYBRID EQUIVALENT MODEL (H-Parameter model)

Here we employ the complete equivalent circuit to show the impact of *hr* and define in more specific terms the impact of *ho*. It is important to realize that since the hybrid equivalent model has the same appearance for the common-base, common-emitter, and common-collector configurations, the equations developed in this section can be applied to each configuration. It is only necessary to insert the parameters defined for each configuration. That is, for a common-base configuration, *hfb*, *hib*, and so on, are employed, while for a common-emitter configuration, *hfe*, *hie*, and so on, are utilized. Recall that Appendix A permits a conversion from one set to the other if one set is provided and the other is required.

Consider the general configuration of Fig. 1 with the two-port parameters of particular interest. The complete hybrid equivalent model is then substituted in Fig. 2 using parameters that do not specify the type of configuration. In other words, the solutions will be in terms of *hi*, *hr*, *hf*, and *ho*.

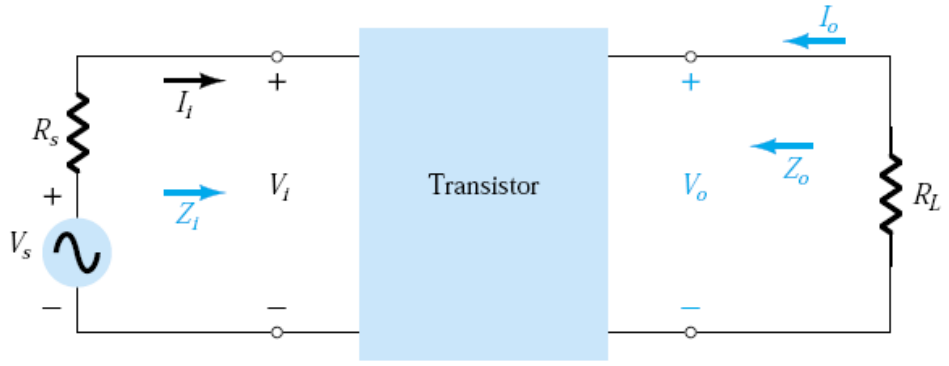


Fig.1 Two-port system.

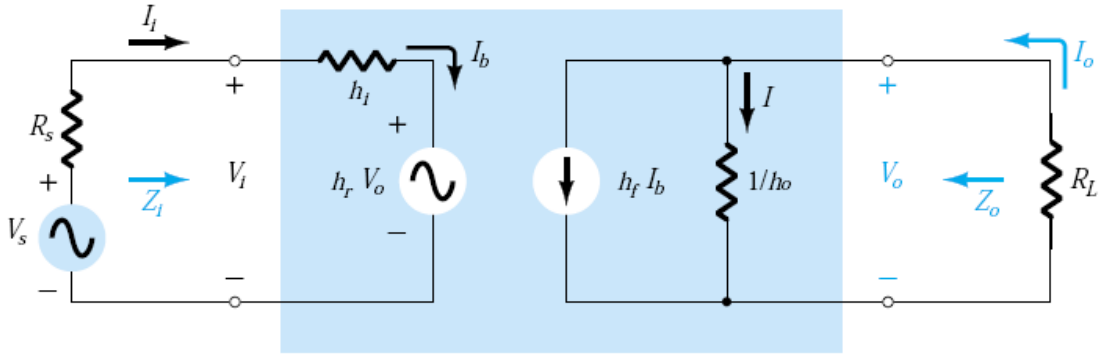


Fig.2 Substituting the complete hybrid equivalent circuit into the two-port system of Fig.1

Current Gain, $A_i = I_o/I_i$

Applying Kirchhoff's current law to the output circuit yields

$$I_o = h_f I_b + I = h_f I_i + \frac{V_o}{1/h_o} = h_f I_i + h_o V_o$$

Substituting $V_o = -I_o R_L$ gives us

$$I_o = h_f I_i - h_o R_L I_o$$

Rewriting the equation above, we have

$$I_o + h_o R_L I_o = h_f I_i$$

and

$$I_o(1 + h_o R_L) = h_f I_i$$

There are two Families of Such Circuits

1. Hybrid- π Model
2. T Model

Hybrid- π Model

Version A

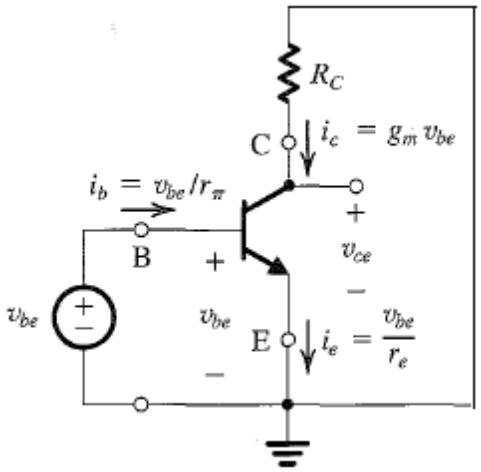


Fig.1 The amplifier circuit of Fig. 5.48(a) with the dc sources (VBE and Vee) eliminated (short circuited). Thus only the signal components are present. Note that this is a representation of the signal operation of the BJT and not an actual amplifier circuit.

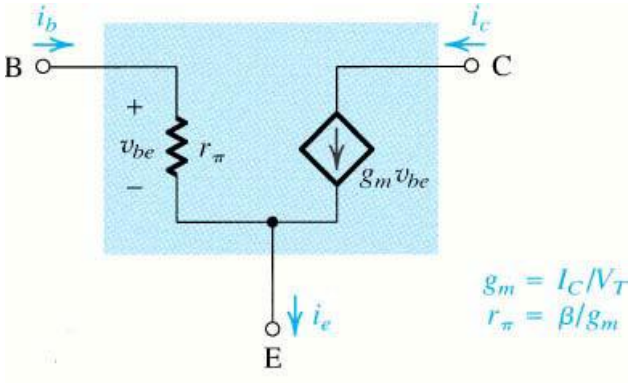


Fig.2 represents the BJT as a voltage-controlled current source (a transconductance amplifier),

An equivalent circuit model for the BJT.is shown in **Fig.2**. This model represents the BJT as a voltage-controlled current source and explicitly includes the input resistance looking into the base, r_π. The model obviously yields $ic = g_m.Vbe$ and $ib = Vbe/ r_\pi$. Not so obvious, however, is the fact that the model also yields the correct expression for i_e. This can be shown as follows:

At the emitter node we have

$$i_e = \frac{Vbe}{r\pi} + gm.Vbe = \frac{Vbe}{r\pi}(1 + gm.r\pi)$$

$$= \frac{Vbe}{r\pi}(1 + \beta) = Vbe/[\frac{r\pi}{1+\beta}]$$

$$ie = Vbe/re$$

Version B

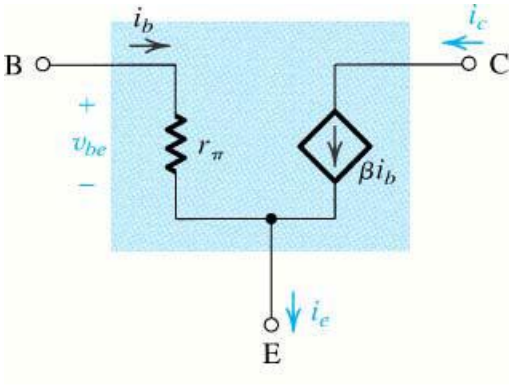


Fig 3. represents the BJT as a current-controlled current source (a current amplifier).

This equivalent circuit model can be obtained by expressing the current of the controlled source (*gm Vbe*) in terms of the base current *ib* as follows:

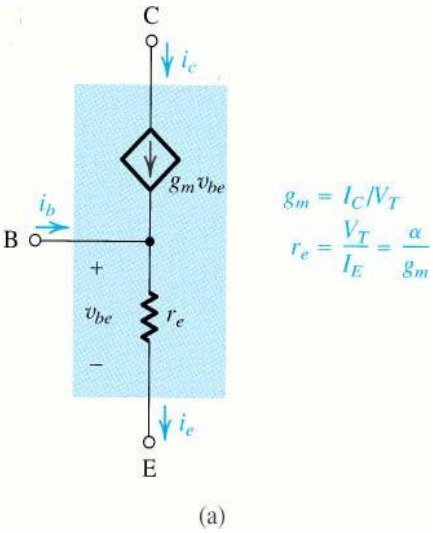
$$gm\,Vbe = gm(ib.r\pi)$$
$$= (gm.r\pi)ib$$
$$= \beta ib$$

Here the transistor is represented as a current-controlled current source, with the control current being ib•

The two models are simplified versions of what is known as the hybrid-π model. This is the most widely used model for the BJT.

T-MODEL

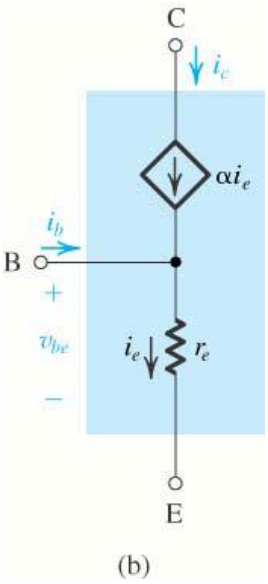
Version A



$$g_m = I_C/V_T$$

$$r_e = \frac{V_T}{I_E} = \frac{\alpha}{g_m}$$

Version B



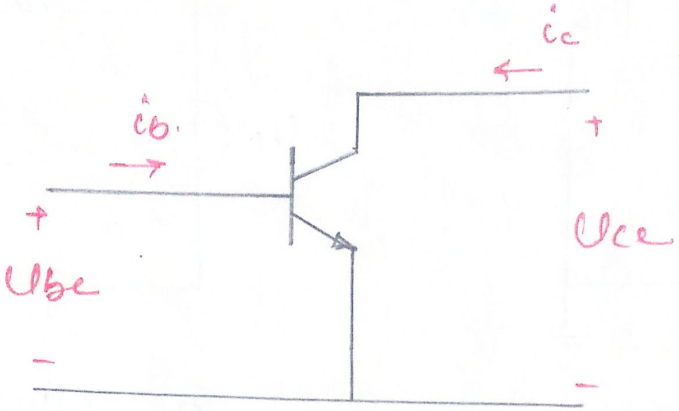
MODULE 2

CS 205

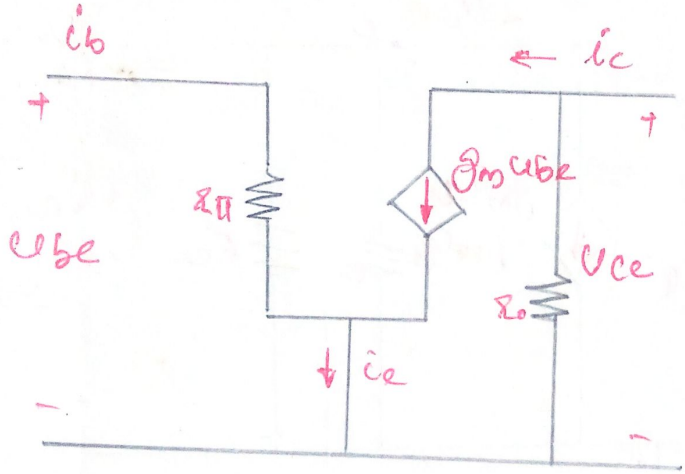
MODULE II

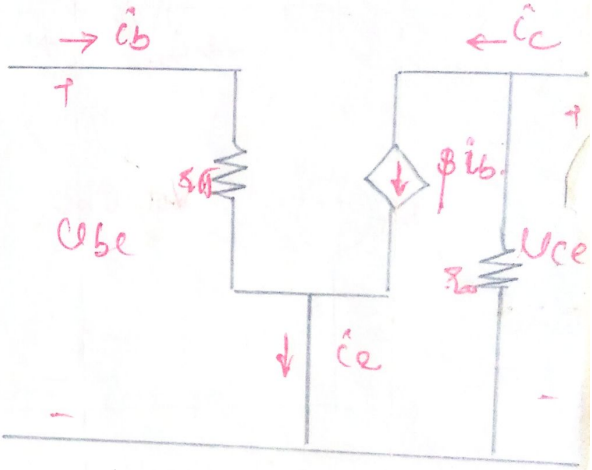
: Small Signal Operation & Models:

Small Signal Hybrid-π Equivalent ckt of BJT.



BJT as Small Signal two-port Network





Small Signal Hybrid π equivalent ckt for npn BJT.

Here $r_\pi = \frac{V_{be}}{i_b} = \frac{V_T}{I_{BQ}} = \frac{\beta V_T}{I_{CQ}}$

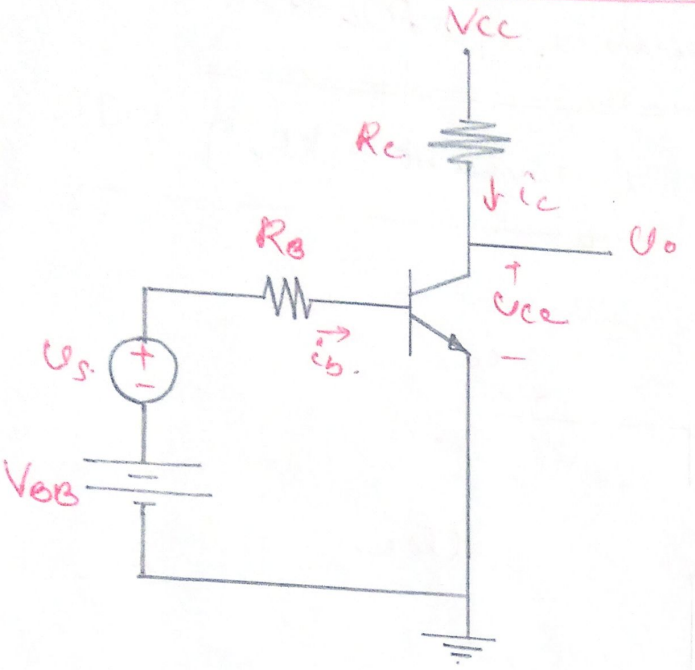
g_m = Trans conductance $= \frac{i_c}{V_T} = \frac{i_c}{V_{be}}$

$g_m V_{be} = \frac{i_c}{V_{be}} \times V_{be} = i_c = \beta i_b$

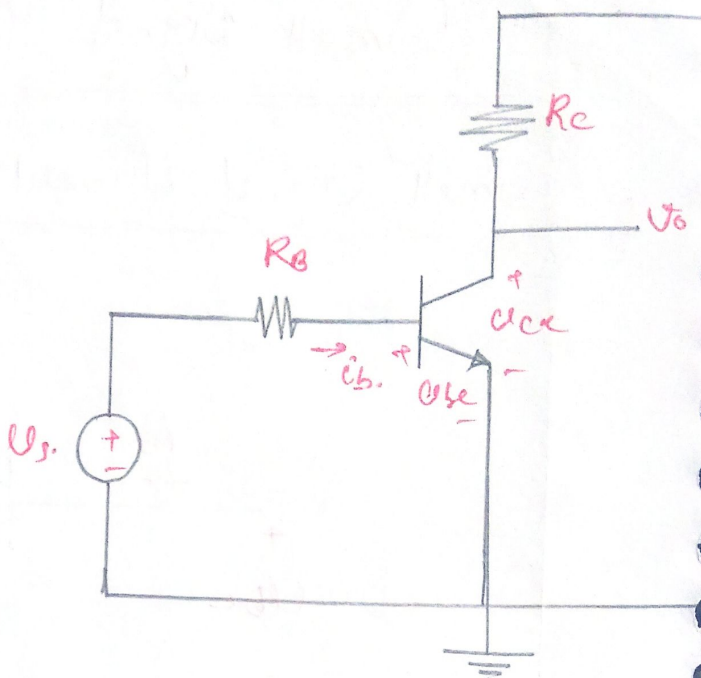
r_o = Small Signal transistor o/p resistance

$= \frac{V_A}{i_c}$; V_A = Early voltage

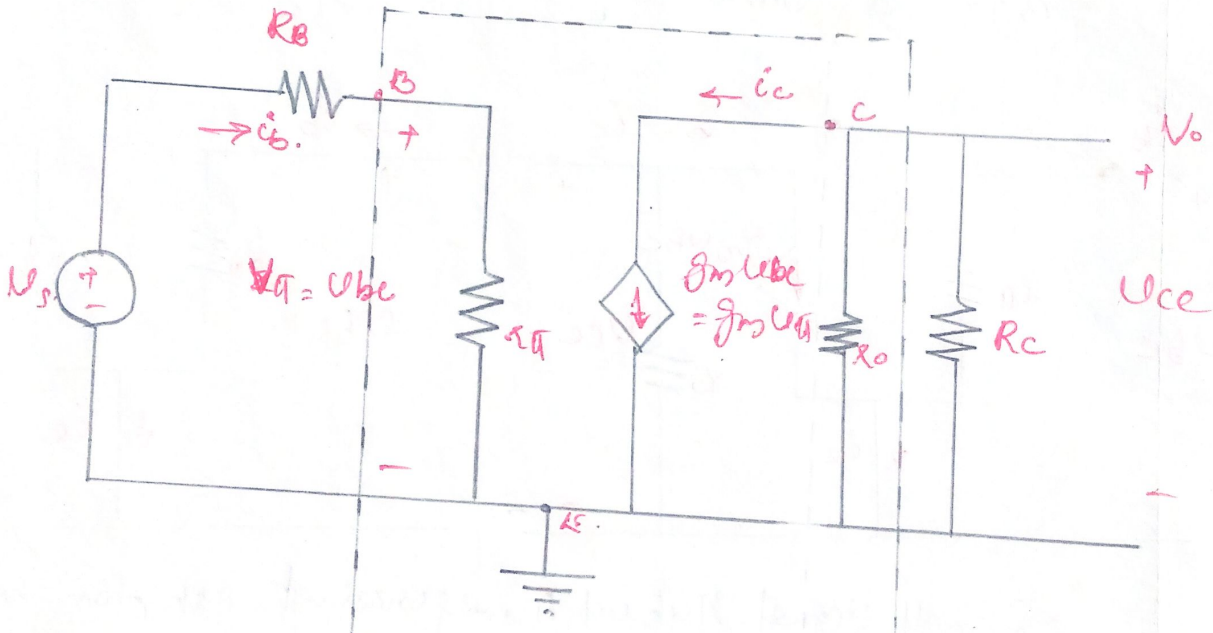
CE - Circuit



CE ckt



DC equivalent circuit.



Small signal equivalent ckt of CE ckt

* Common Emitter Current gain.

$$\frac{i_c}{i_b} = \frac{g_m V_{be}}{V_{be}/r_\pi} = g_m r_\pi = \frac{i_c}{V_{be}} \times \frac{V_{be}}{i_b}$$

$$= \frac{\beta i_b}{i_b}$$

$$= \beta$$

Small Signal Voltage gain.

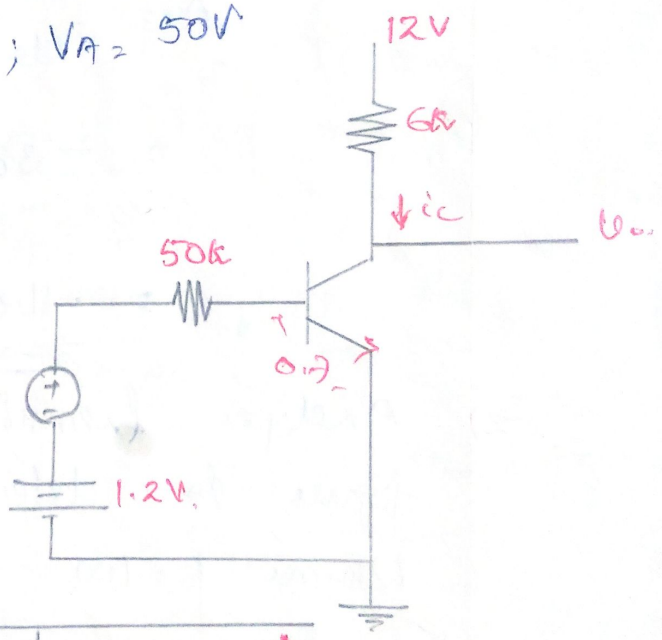
$A_V = V_o / V_s$.

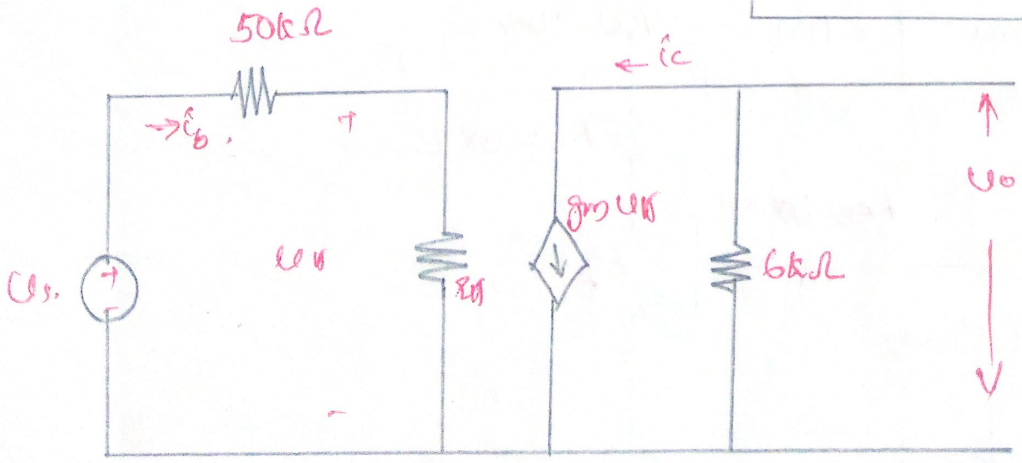
$V_o = -g_m V_\pi \times R_C$ & $V_\pi = V_s \times \frac{r_\pi}{r_\pi + R_B}$.

$\therefore V_o = -g_m \cdot V_s \left(\frac{r_\pi}{r_\pi + R_B}\right) \cdot R_C$

$A_V = \frac{V_o}{V_s} = -g_m R_C \cdot \frac{r_\pi}{r_\pi + R_B}$.

Prblm: Calculate small signal voltage gain of BJT ckt shown in figure. Assume hybrid-π parameters as: $\beta = 100$; $V_{CC} = 12V$; $V_{BE} = 0.7V$; $R_C = 6k\Omega$, $R_B = 50k\Omega$; $V_{BB} = 1.2V$.; $V_A = 50V$





& Small signal parameters

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$$r_\pi = \frac{\beta V_T}{I_{CQ}}$$

$$g_m = \frac{I_{CQ}}{V_T}$$

From DC analysis

$$V_{BB} - I_B R_B - 0.7 = 0$$

$$I_{BQ} = \frac{1.2 - 0.7}{50k} = 10\mu A$$

$$I_{CQ} = \beta I_{BQ} = 1mA$$

$$r_\pi = \frac{100 \times 0.026}{1m} = 2.6k\Omega$$

$$r_o = \frac{V_A}{I_{CQ}} = \frac{50}{1mA} = 50k\Omega$$

$$g_m = \frac{1m}{26m} = 38.46 mA/V$$

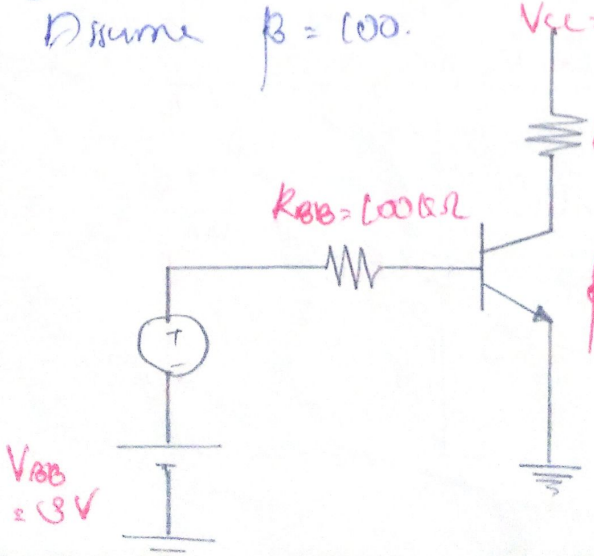
Small signal voltage gain

$$A_v = \frac{V_o}{V_s} = -g_m R_c \left(\frac{r_\pi}{r_\pi + R_B}\right)$$

$$= -38.46m \times 6k \times \left(\frac{2.6k}{2.6k + 50k}\right)$$

$$= -11.4$$

2) Analyze transistor amplifier shown in figure to determine its voltage gain. Assume $\beta = 100$.



$$V_{BB} - I_B R_B - V_{BE} = 0.$$

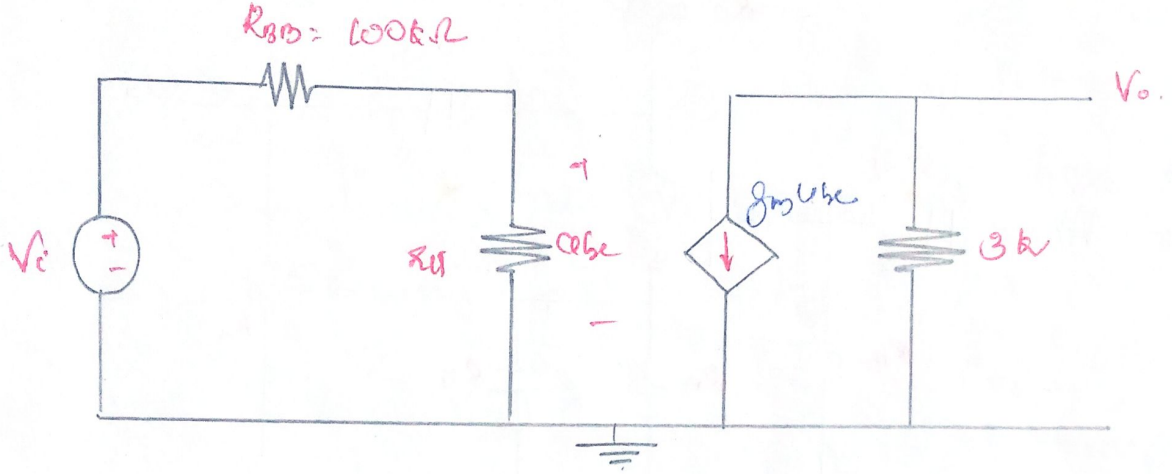
$$I_{B_Q} = \frac{V_{BB} - V_{BE}}{R_B} = \frac{3 - 0.7}{100k}$$

$$= 23\,\mu A \qquad I_{CQ} = 2.3\,mA$$

$$V_{CC} - I_C R_L - V_{CE} = 0$$

$$V_{CE_Q} = 10 - 2.3m \times 3k$$

$$= 3.1\,V$$



$$g_m = \frac{I_C}{V_T} = \frac{2.3m}{26m} = 88.46\,mA/V$$

$$r_\pi = \frac{\beta V_T}{I_{CQ}} = \frac{100 \times 26m}{2.3mA} = 1.13\,k\Omega$$

$$A_V = \frac{V_o}{V_i};$$

$$V_o = -2.966\,V_i$$

$$A_V = \frac{V_o}{V_i} = -2.966$$

-ve sign indicates phase reversal

$$V_o = -g_m V_{be} \times 3k$$

$$V_{be} = V_i \times \frac{r_\pi}{r_\pi + 100k}$$

$$= V_i \times \frac{1.13k}{1.13k + 100k}$$

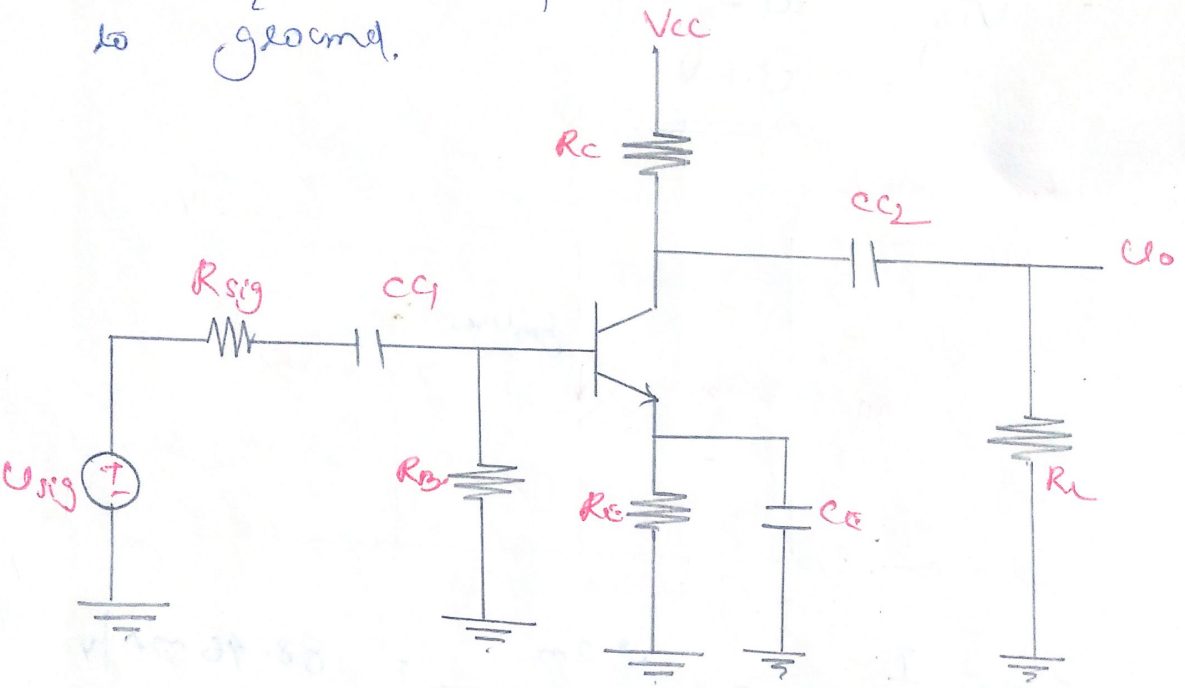
$$= 0.011780$$

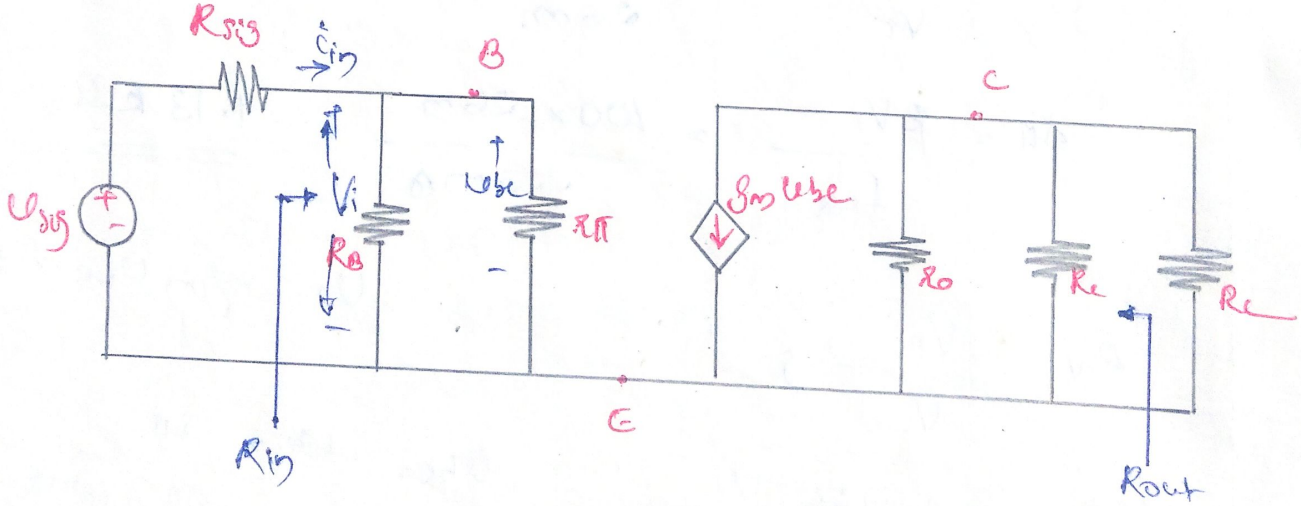
$$= 0.01118\,V_i$$

$$V_o = -2.966\,V_i$$

Common Emitter (CE) Amplifier

The CE configuration is the most widely used of all BJT amplifier circuits. The emitter bypass capacitor C_E connected between emitter and ground. This capacitor is required to provide a very low impedance to ground.





Equivalent ckt obtained by replacing the transistor with its hybrid π model.

To determine the terminal characteristics of CE amplifier, i.e its input impedance, o/p impedance & voltage gain; replace BJT with its hybrid-π small signal model.

Input resistance R_{in}.

$$R_{in} = \frac{V_{in}}{i_{in}} = R_B \| r_\pi$$

R_{in} of CE amplifier will be a few kilo ohms.

Voltage gain (A_V)

The fraction of source signal V_{sig} that appears across input terminal of BJT i.e V_i

$$V_i = V_{sig} \times \frac{R_{in}}{R_{in} + R_{sig}} = V_{sig} \times \frac{(R_B \| r_\pi)}{(R_B \| r_\pi) + R_{sig}}$$

when $R_B >> r_\pi$ $\therefore$ R_B can be neglect

$$\therefore V_i = V_{sig} \frac{r_\pi}{r_\pi + R_{sig}}$$

$$V_{be} = V_i$$

At o/p side $V_o = -g_m V_{be} (r_o \| R_c \| R_L)$

$$= -g_m V_i (r_o \| R_c \| R_L)$$

$$\therefore \boxed{A_V = -g_m (r_o \| R_c \| R_L)}$$

Sol: for V_i defining $A_V = \frac{V_o}{V_{sig}}$

Open ckt voltage gain can be found be setting $R_L = \infty$

$$\boxed{A_{Vo} = -g_m (r_o \| R_c)}$$

Since $r_o >> R_c$

$$A_{v_0} = -g_m R_c$$

O/p resistance

The o/p resistance R_{out} can be found from equivalent ckt by looking back into o/p terminals while short circuiting the source sig.

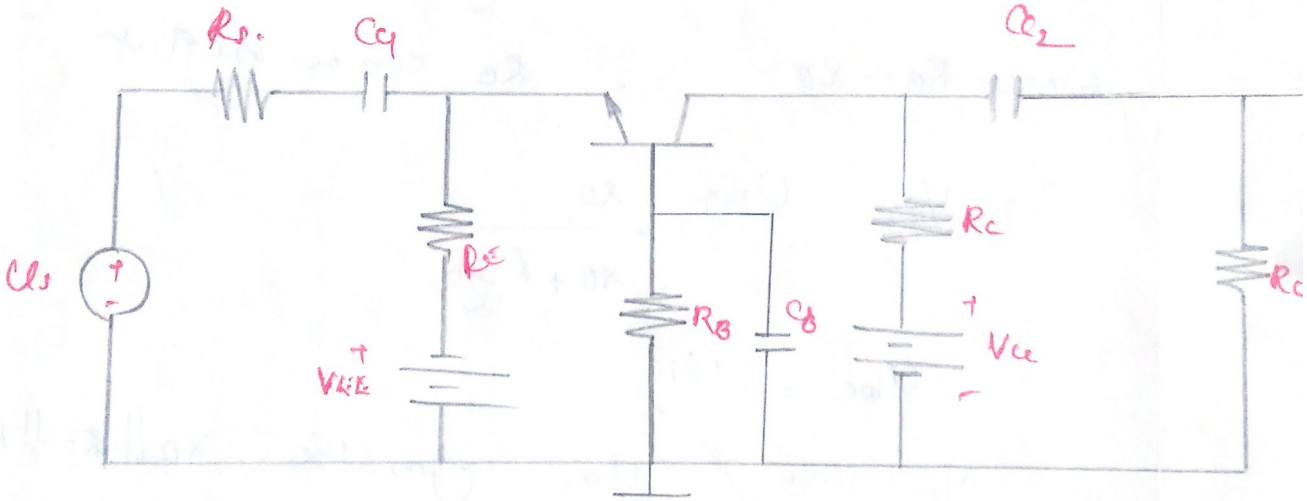
$\therefore V_i = V_{sc} = 0.$

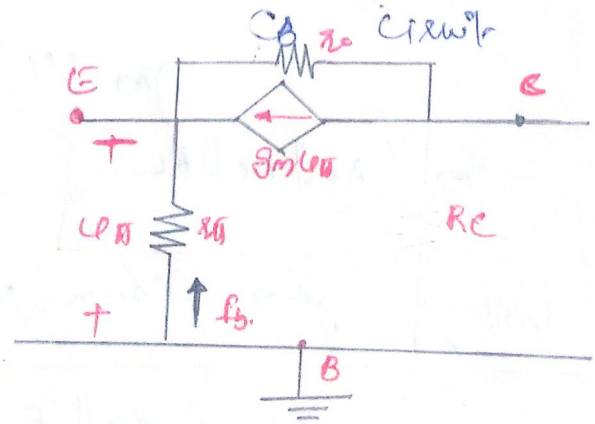
$$\therefore \boxed{R_{out} = R_c \| r_o} \qquad R_c \| r_o.$$

$\therefore r_o >> R_c$

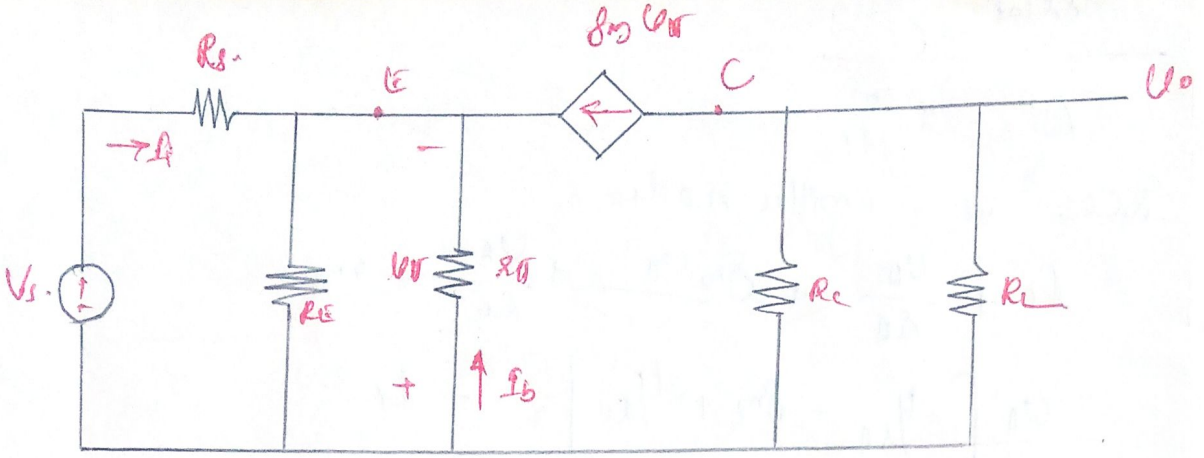
$$R_{out} \simeq R_c$$

: Common Base Amplifier :





Hybrid-π equivalent for CB ckt



Small signal equivalent ckt of CB amp

Here hybrid-π model of npn transistor with o/p resistance r_o assumed to be infinite

Voltage Gain

KCL at emitter node

$$g_m v_\pi + \frac{v_\pi}{r_\pi} + \frac{v_\pi}{R_E} + \frac{v_s - (-v_\pi)}{R_s} = 0.$$

$\beta = g_m r_\pi$

$$\frac{g_m v_\pi r_\pi + v_\pi}{r_\pi} + \frac{v_\pi}{R_E} + \frac{v_s + v_\pi}{R_s} = 0.$$

$$v_\pi \left[\frac{\beta+1}{r_\pi} + 1/R_c + 1/R_s \right] = -\frac{v_s}{R_s}.$$

$$v_o = \frac{-v_s}{R_s} \left[\frac{r_\pi}{\beta+1} \parallel R_c \parallel R_s \right] \quad \text{---} (1)$$

$$v_o = -g_m v_\pi (R_c \parallel R_L) \quad \text{---} (2)$$

Substitute eqn (1) in (2)

$$v_o = \frac{g_m v_s}{R_s} \left[\frac{r_\pi}{\beta+1} \parallel R_c \parallel R_s \right] (R_c \parallel R_L)$$

$$\boxed{A_v = \frac{v_o}{v_s} = g_m \frac{(R_c \parallel R_L)}{R_s} \left[\frac{r_\pi}{\beta+1} \parallel R_E \parallel R_s \right]}$$

when $R_s \to 0$; $A_v = g_m (R_c \parallel R_L)$

Current gain:

$A_i = I_o / I_i$

KCL at emitter node

$$I_i + \frac{V_\pi}{r_\pi} + g_m V_\pi + \frac{V_\pi}{R_E} = 0.$$

$$V_\pi \left[1/r_\pi + g_m + 1/R_E \right] = -I_i$$

$$V_\pi \left[\frac{1+\beta}{r_\pi} + 1/R_E \right] = -I_i$$

$$V_\pi = -I_i \left[\frac{r_\pi}{\beta+1} \parallel R_E \right] \quad \text{---- (3)}$$

Load current $I_o = -g_m V_\pi \left(\frac{R_c}{R_c + R_L} \right)$ ---- (4)

Sub: (3) in (4) $\Rightarrow$

$$I_o = -g_m \times -I_i \left[\frac{r_\pi}{\beta+1} \parallel R_E \right] \left[\frac{R_c}{R_c + R_L} \right]$$

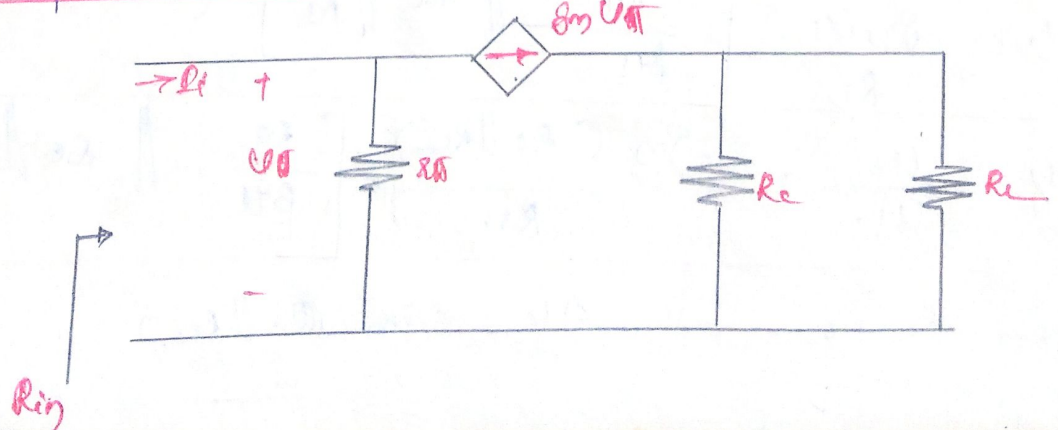
$$A_I = \frac{I_o}{I_i} = g_m \left(\frac{R_c}{R_c + R_L} \right) \left(\frac{r_\pi}{1+\beta} \parallel R_E \right)$$

when $R_E \to \infty$ and $R_L = 0$.

$A_{io} = \frac{g_m r_\pi}{1+\beta} = \frac{\beta}{1+\beta} = \alpha$ (approx)

where α = Common base Current gain.

Input & Output impedances:



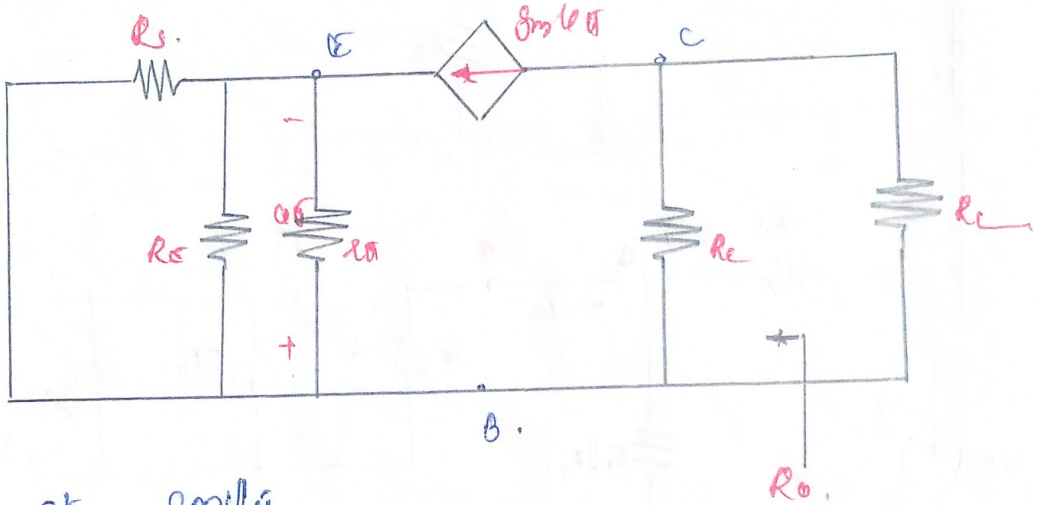
$R_i = \frac{V_\pi}{I_i}$

KCL at input $I_i = I_b + g_m V_\pi = \frac{V_\pi}{r_\pi} + g_m V_\pi$

$= V_\pi \left(\frac{1+\beta}{r_\pi}\right)$

$$R_i = \frac{V_\pi}{I_i} = \frac{r_\pi}{1+\beta} \simeq R_e.$$

O/p impedance



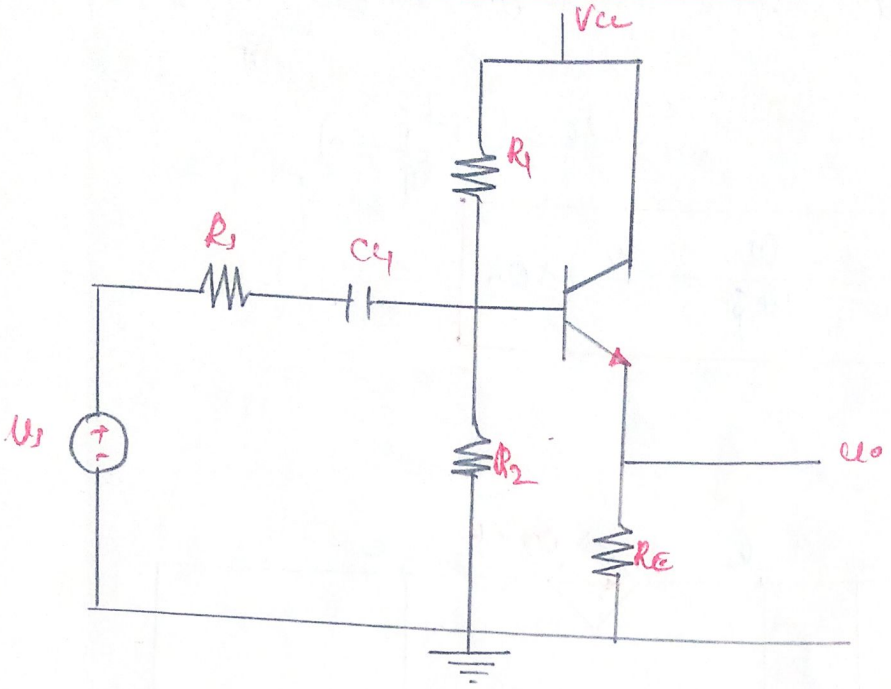
KCL at emitter

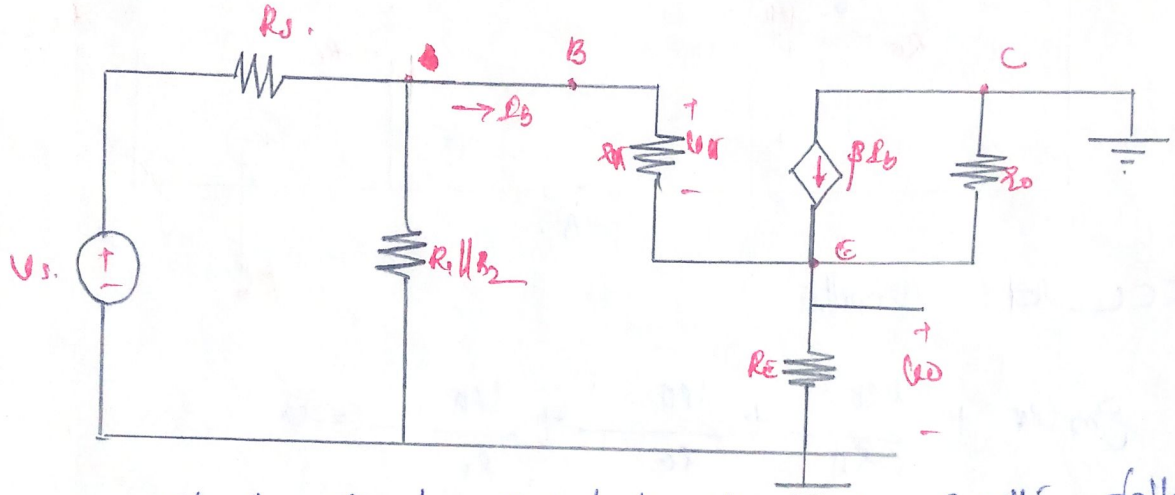
$$g_m V_\pi + \frac{V_\pi}{r_\pi} + \frac{V_\pi}{R_E} + \frac{V_\pi}{R_s} = 0$$

when $V_\pi = 0$: $g_m V_\pi = 0$.

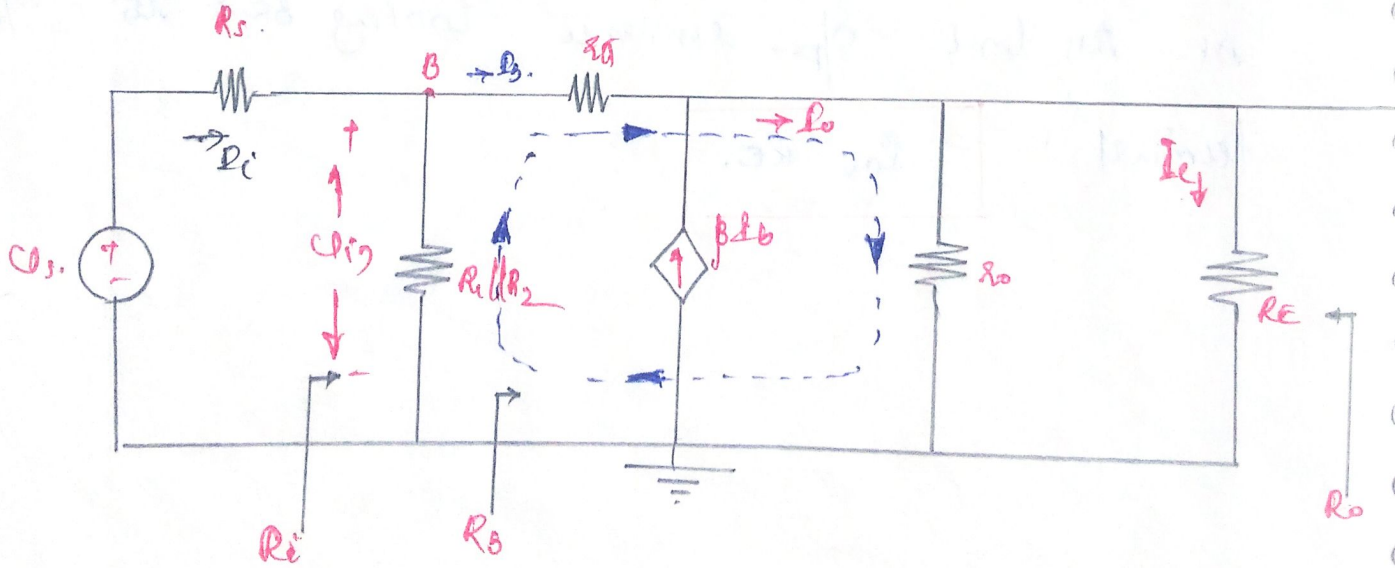
Thus the o/p resistance looking back to o/p terminal $R_o = R_e$.

Common Collector [Emitter - follower] Amplifier





Small signal equivalent ckt of emitter follower



Small signal equivalent with all grounds connected together

Voltage gain

From figure $I_o = I_E = (\beta+1) I_b$.

O/p voltage $V_o = (\beta+1) I_b (r_o \| R_E)$ ---- (1)

writing KVL around base-emitter loop

$$V_{in} - I_b r_\pi - (\beta+1) I_b (r_o \| R_E) = 0.$$

$$V_{in} = I_b [r_\pi + (\beta+1)(r_o \| R_E)] \quad \text{--- (2)}$$

or

$$R_{ib} = \frac{V_{in}}{I_b} = r_\pi + (\beta+1)(r_o \| R_E)$$

$$V_{in} = \left(\frac{R_i}{R_i + R_s}\right) V_s \quad \text{---------- (3)}$$

$$\boxed{R_i = R_1 \| R_2 \| R_{ib}}$$

$$V_s = V_{in} \cdot \left(\frac{R_i + R_s}{R_i}\right) \quad \text{--- (4)}$$

$$\therefore \frac{V_o}{V_s} = A_V = \frac{(\beta+1) I_b (r_o \| R_E)}{\frac{R_i + R_s}{R_i} \cdot V_{in}}$$

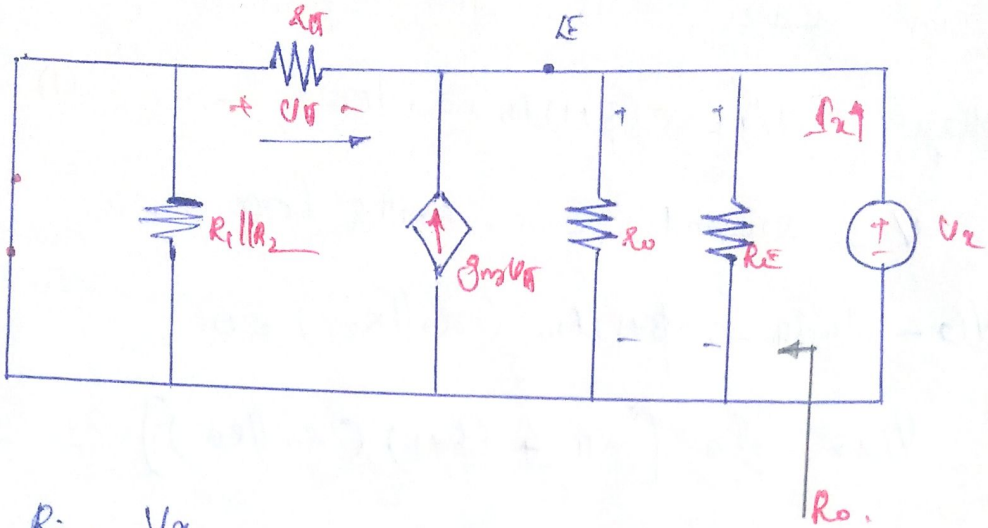
$$A_V = \frac{(1+\beta)(r_o \| R_E) I_b}{V_{in}} \times \frac{R_i}{R_i + R_s}$$

Sub V_{in} from eq (2)

$$A_V = \frac{(1+\beta)(r_o \| R_E) I_b}{I_b (r_\pi + (1+\beta)(r_o \| R_E))} \times \frac{R_i}{R_i + R_s}$$

$$\boxed{A_V = \frac{(1+\beta)(r_o \| R_E)}{r_\pi + (1+\beta)(r_o \| R_E)} \cdot \frac{R_i}{R_i + R_s}} \quad \text{--- (5)}$$

O/p impedance



$$R_o = \frac{V_x}{I_x} \qquad \text{from figure } V_\pi = -V_x$$

KCL at o/p node

$$I_x + g_m v_\pi + \frac{v_\pi}{r_\pi} = \frac{v_x}{r_o} + \frac{v_x}{R_E}$$

$\therefore v_\pi = -v_x$

$$I_x + g_m(-v_x) = \frac{v_x}{r_o} + \frac{v_x}{R_E} + \frac{v_x}{r_\pi} + g_m v_x \quad \text{---(6)}$$

$$I_x = v_x \left[1/r_o + 1/R_E + \frac{1}{r_\pi} + g_m \right]$$

$$\boxed{R_o = \frac{v_x}{I_x} = 1/g_m \| r_o \| R_E \| r_\pi} \quad \text{---(7)}$$

from eqn (6)

$$\frac{I_x}{v_x} = \frac{1}{R_o} = g_m + \frac{1}{r_\pi} + \frac{1}{r_o} + \frac{1}{R_E}$$

$$= \frac{g_m r_\pi + 1}{r_\pi} + \frac{1}{r_o} + \frac{1}{R_E}$$

$$= \frac{\beta + 1}{r_\pi} + 1/r_o + \frac{1}{R_E}$$

$$\boxed{R_o = \frac{r_\pi}{\beta + 1} \| r_o \| R_E}$$

Current gain

$$A_i = \frac{I_e}{I_i}$$

Using current division rule

$$I_b = \frac{R_1 \| R_2}{(R_1 \| R_2 + R_{ib})} I_i$$

Since $I_{emitter} = \beta I_b$

$$I_o = I_b + \beta I_b = (1+\beta) I_b = (1+\beta) \left(\frac{R_1 \| R_2}{R_1 \| R_2 + R_{ib}} \right) I_i \quad \text{---(1)}$$

$$I_e = \frac{r_o}{(r_o + R_E)} \times I_o \quad \text{---(2)}$$

Substitute (1) in (2)

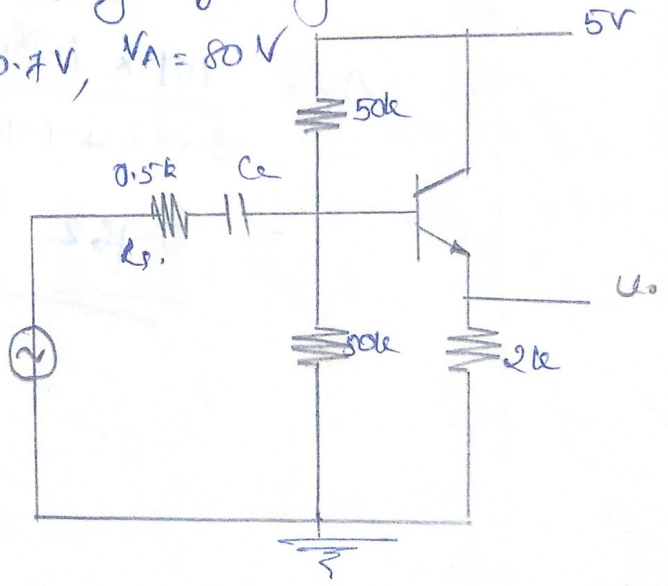
$$I_e = (1+\beta) \left(\frac{R_1 \| R_2}{R_1 \| R_2 + R_{ib}} \right) I_i \times \frac{r_o}{r_o + R_E}$$

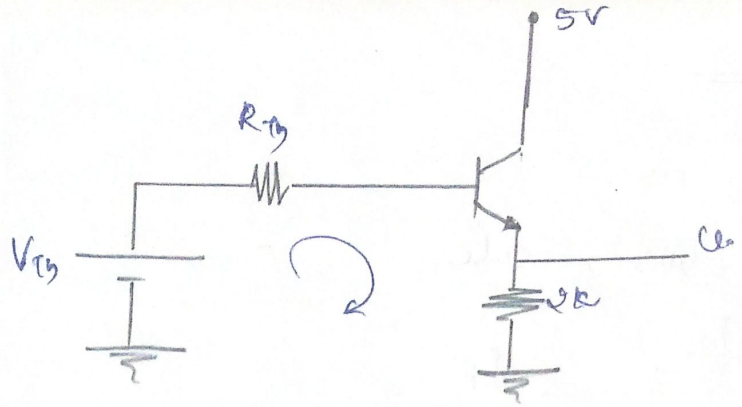
$$A_i = \frac{I_e}{I_i} = (1+\beta) \left(\frac{R_1 \| R_2}{R_1 \| R_2 + R_{ib}} \right) \left(\frac{r_o}{r_o + R_E} \right)$$

If we assume $R_1 \| R_2 >> R_{ib}$ & $r_o >> R_E$

Then $A_i \simeq (1+\beta)$

Prblm: Calculate small signal voltage gain of an emitter follower :- $\beta = 100$, $V_{BE} = 0.7\,V$, $V_A = 80\,V$





$V_{Th} = 2.5V$

$R_{Th} = 25k$

$V_{Th} - I_{BQ} R_{Th} - 0.7 - I_{BQ}(\beta+1).2k = 0.$

$(25k + 101 \times 2k) I_{BQ} = 2.5 - 0.7$

$I_{BQ} = \frac{1.8}{227k} = 7.929\mu A$

$I_{CQ} = \beta I_{BQ} = 0.793mA$

$r_\pi = \frac{V_T \beta}{I_{CQ}} = \frac{26m \times 100}{0.793m} = 3.28k\Omega$

$g_m = \frac{I_{CQ}}{V_T} = 30.5mA/V$

$r_o = \frac{V_A}{I_{CQ}} = 100.88k\Omega.$

$A_V = \frac{(1+\beta)(r_o \| R_E)}{r_\pi + (1+\beta)(r_o \| R_E)} \cdot \frac{R_i}{R_i + R_s}$ ---- (1)

$R_i = R_1 \| R_2 \| R_{ib} = 22.2k\Omega$

$R_{ib} = r_\pi + (\beta+1)(r_o \| R_E) = 198.k\Omega + 3.28k = 201.35k$

$\therefore A_V = \frac{101 \times 1.96k}{3.28k + 101 \times 1.96k} \times \frac{22.2k}{22.2k + 0.5k}$

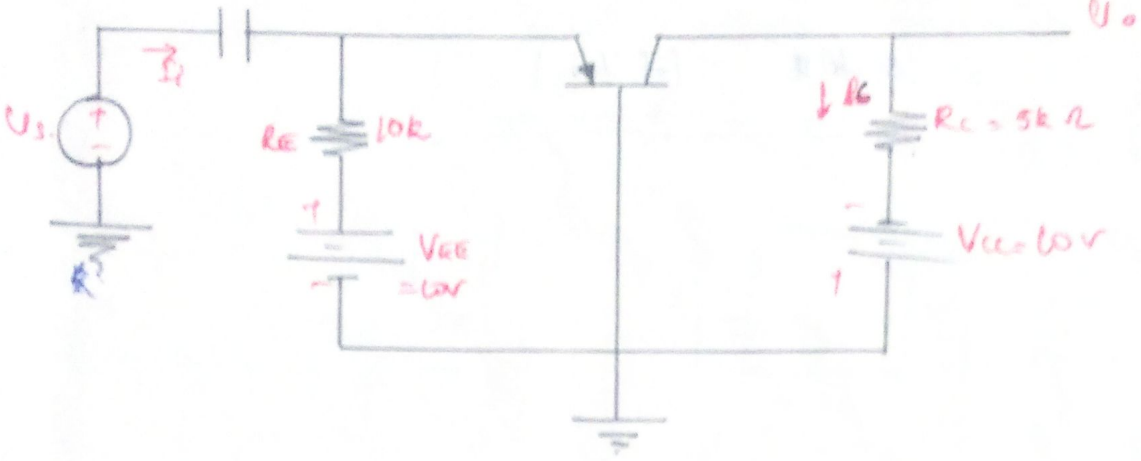
$= 0.962$

Prblm: For the CB circuit shown, the transistor parameters are calculate

$\beta = 100$; $V_{BE(ON)} = 0.7V$ and $R_o = \infty$.

(a) Quiescent values of I_{CQ} and V_{CEQ}

(b) Determine A_i, A_v,



KVL at input side

$$10 - (\beta+1) I_B \times 10k - 0.7 = 0.$$

$$I_B = \frac{10 - 0.7}{(\beta+1)10k} = 9.21\ \mu A$$

$$I_{CQ} = 0.921\ mA$$

Again KVL around CE;

$$10 - (\beta+1) I_B \times 10k - V_{CE} - I_C R_C + 10 = 0.$$

$$V_{CEQ} = 6.092\ V$$

$$A_i = g_m \left(\frac{R_C}{R_C + R_L}\right)\left(\frac{R_\pi}{1+\beta} \parallel R_E\right)$$

$$A_v = g_m \left(\frac{R_C \parallel R_L}{R_s}\right)\left[\frac{R_\pi}{\beta+1} \parallel R_E \parallel R_s\right]$$

When $R_s \to 0$

$$A_v = (g_m (R_C \parallel R_L))$$

$$= g_m R_C$$

$$R_\pi = \frac{V_T \beta}{I_{CQ}} = \frac{26m \times 100}{0.921m} = 2.823k\Omega$$

$$g_m = \frac{I_{CQ}}{V_T} = 35.92\ mA/V$$

$A_i = 35.42m\,(1) \cdot \frac{2.823K}{101} // 10K$

$= 0.987$

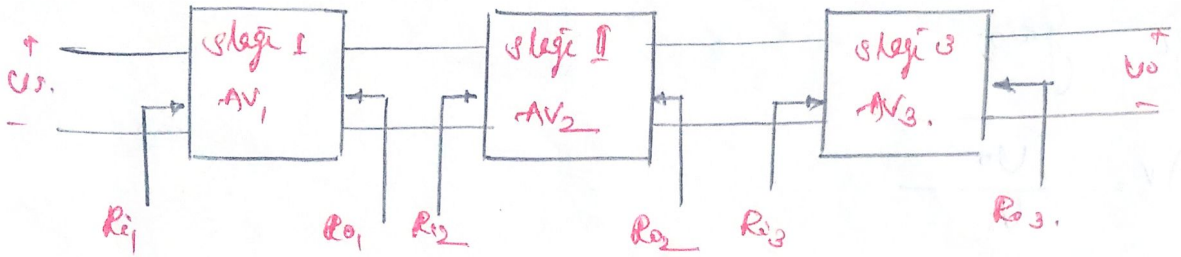
$A_v = g_m R_c$

$= 35.42m \times 5K\Omega$

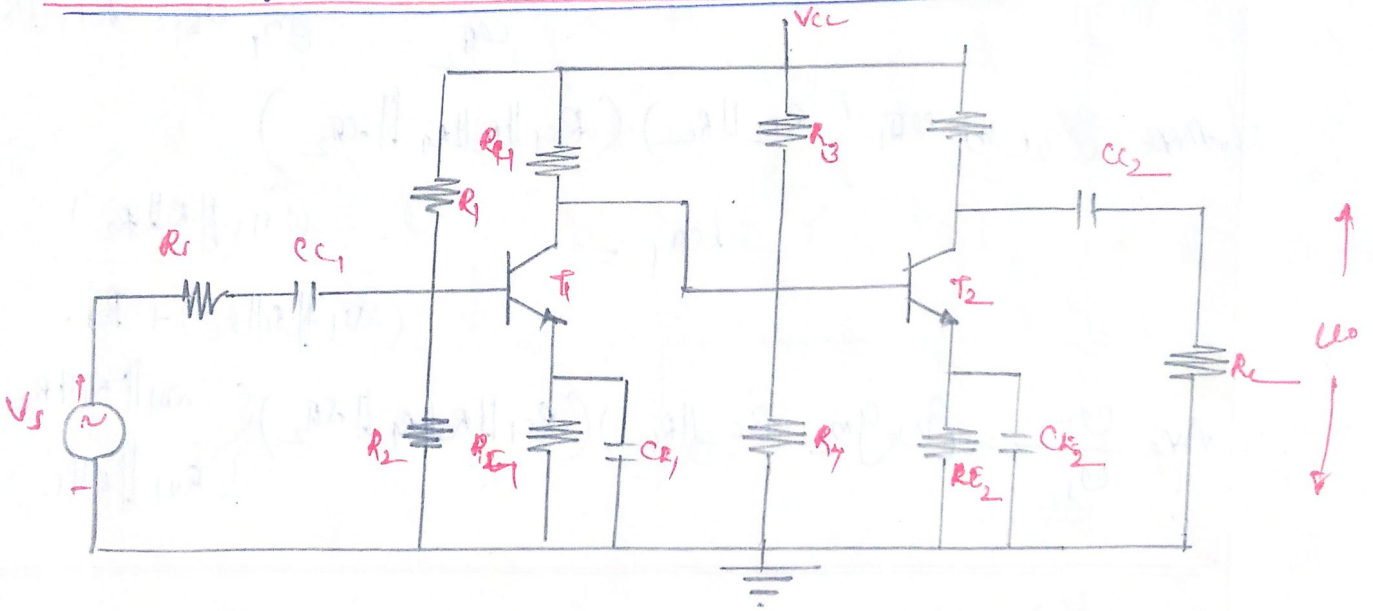
$= 177.1$

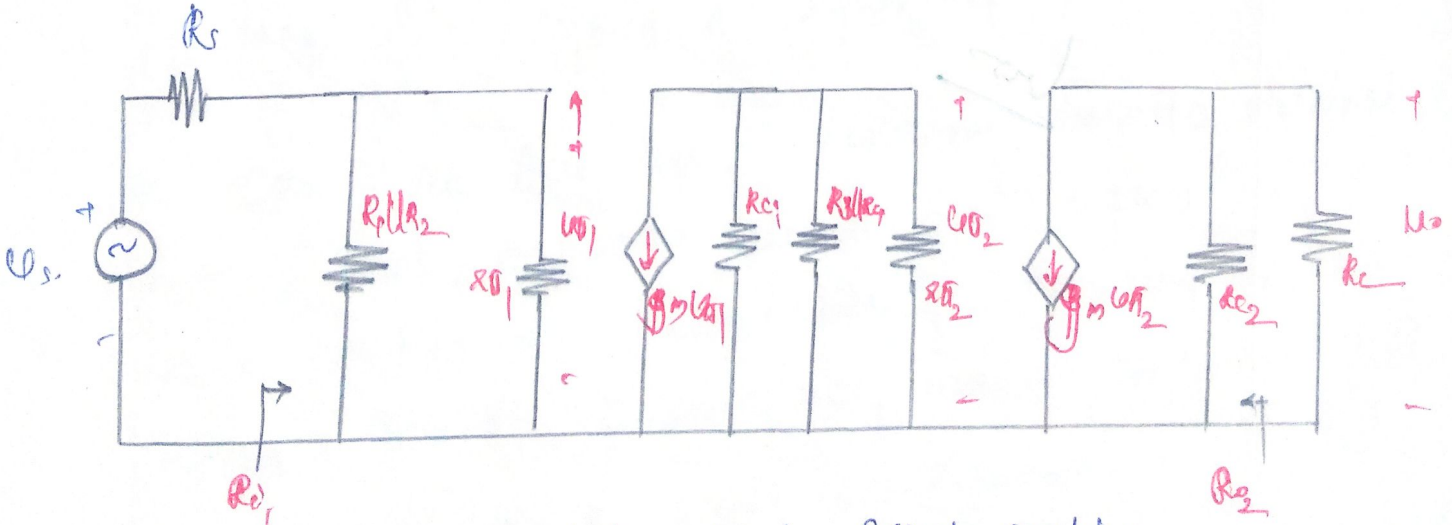
: Multistage Amplifiers :

In most applications, a single transistor amplifier will not be able to meet the specifications of given amplification factor, input & o/p impedances etc. These specifications can be met by the use of multistage amplifiers.



: Multistage Analysis : Cascade Configuration :





Small signal equivalent ckt of cascade amplifier

Input impedance

It is the impedance which can be seen looking into the input terminal of 1st stage of amplifier.

Here

$$R_i = R_1 \| R_2 \| R_{\pi 1}$$

O/p impedance

$$R_o = R_{C_2}$$

Voltage gain

$$A_v = \frac{v_o}{v_s}$$

$$v_o A_v = -g_{m_2} v_{\pi_2} (R_{C_2} \| R_L) \quad \text{-----(1)}$$

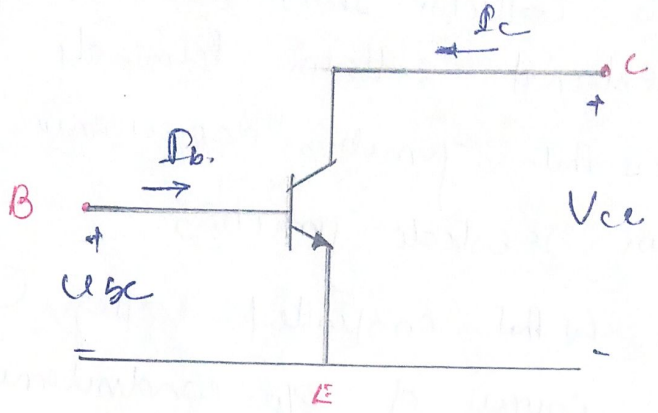
$$v_{\pi_2} = -g_{m_1} v_{\pi_1} \cdot R_{C_1} \| R_{B_3} \| R_{B_4} \| R_{\pi_2}$$

$$\therefore v_o A_v = g_{m_2} g_{m_1} v_{\pi_1} (R_{C_2} \| R_L)(R_{C_1} \| R_{B_3} \| R_{B_4} \| R_{\pi_2})$$

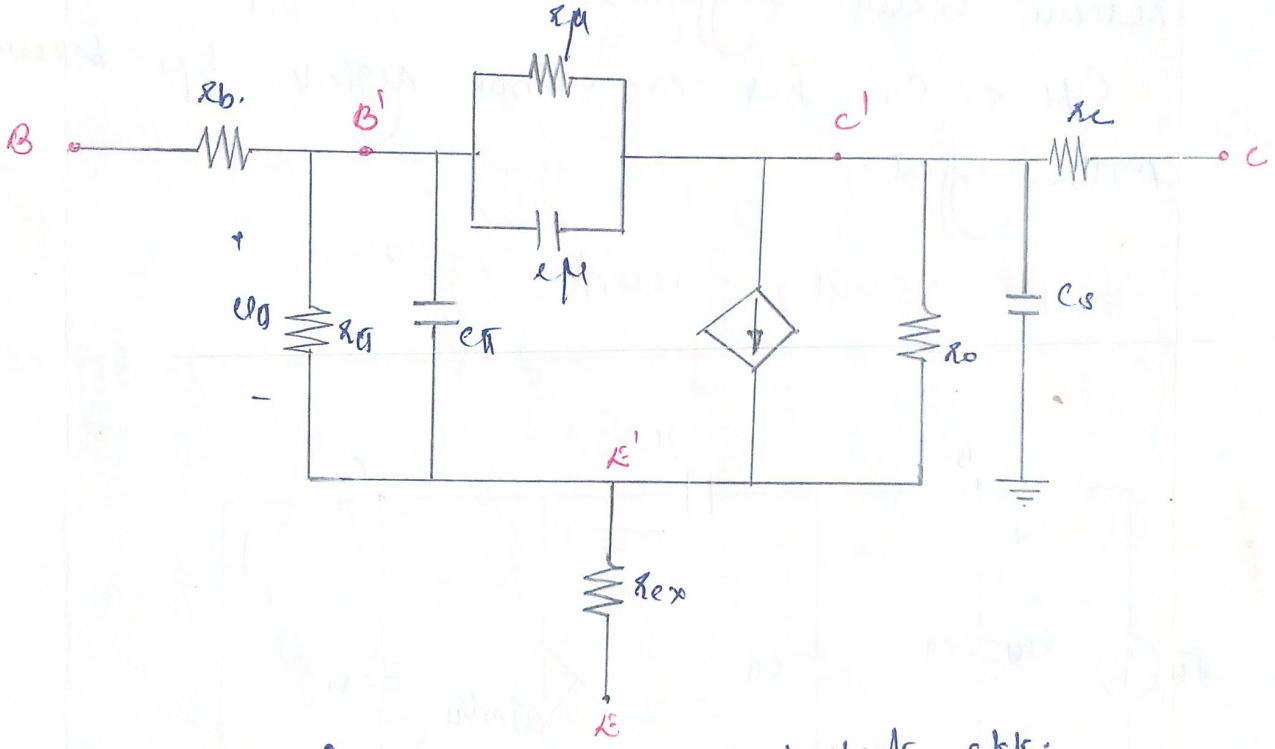
$$v_{\pi_1} = \frac{v_s \cdot (R_{\pi_1} \| R_1 \| R_2)}{(R_{\pi_1} \| R_1 \| R_2) + R_s}$$

$$\therefore A_v = \frac{v_o}{v_s} = g_{m_1} g_{m_2} (R_{C_2} \| R_L)(R_{C_1} \| R_{B_3} \| R_{B_4} \| R_{\pi_2}) \left(\frac{R_{\pi_1} \| R_1 \| R_2}{(R_{\pi_1} \| R_1 \| R_2) + R_s} \right)$$

Hybrid - π Equivalent ckt [High frequency].



CE npn transistor with small signal currents and voltages.



High freq Hybrid π equivalent ckt.

rb is the base series resistance between external base terminal B and internal base region B'. B'-E' junction is forward biased. So cπ is the forward biased junction capacitance and rπ is the forward biased junction resistance.

r_{ex} is the emitter series resistance between external emitter terminal and internal emitter region.

r_c is collector series resistance between internal and external collector terminals.

C_s is the junction capacitance of reverse biased collector - substrate junction.

$g_m v_{\pi}$ is the controlled voltage source

r_o is inverse of o/p conductance g_o.

Since B'C junction is reverse biased C_μ is the junction capacitance of B'C junction. r_μ is the reverse biased diffusion resistance (r_μ is in MΩ)

$C_\mu << C_\pi$ but we cannot neglect C_μ because of Miller effect.

Short - Circuit Current Gain:

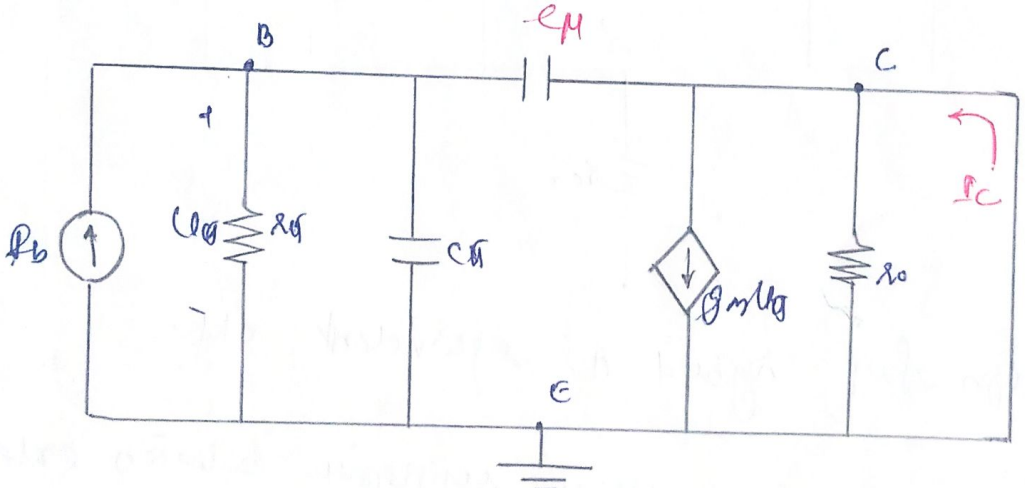


Figure shows simplified hybrid π model for transistor with neglecting r_b, r_c, r_{ex}, r_μ & C_s.

Short circuit current gain

$$A_i = \frac{I_c}{I_b}.$$

KCL at input node

$$I_b = \frac{V_\pi}{r_\pi} + \frac{V_\pi}{1/j\omega C_\pi} + \frac{V_\pi}{1/j\omega C_\mu}$$

$$I_b = V_\pi \left[1/r_\pi + j\omega (C_\pi + C_\mu) \right] \quad \text{--- (1)}$$

KCL at o/p node;

$$\frac{V_\pi}{1/j\omega C_\mu} + I_c = g_m V_\pi$$

$$I_c = V_\pi (g_m - j\omega C_\mu) \quad \text{---- (2)}$$

$$V_\pi = \frac{I_c}{g_m - j\omega C_\mu}$$ sub. in eqn (1)

$$I_b = \frac{I_c \left[1/r_\pi + j\omega (C_\pi + C_\mu) \right]}{(g_m - j\omega C_\mu)}$$

$$A_i = \frac{I_c}{I_b} = h_{fe} = \frac{g_m - j\omega C_\mu}{1/r_\pi + j\omega (C_\pi + C_\mu)}$$

$$A_i = h_{fe} \cong \frac{g_m}{1/r_\pi + j\omega (C_\pi + C_\mu)} \quad \because \omega C_\mu << g_m$$

$$\boxed{A_i = h_{fe} = \frac{g_m r_\pi}{1 + j\omega r_\pi (C_\pi + C_\mu)}}$$

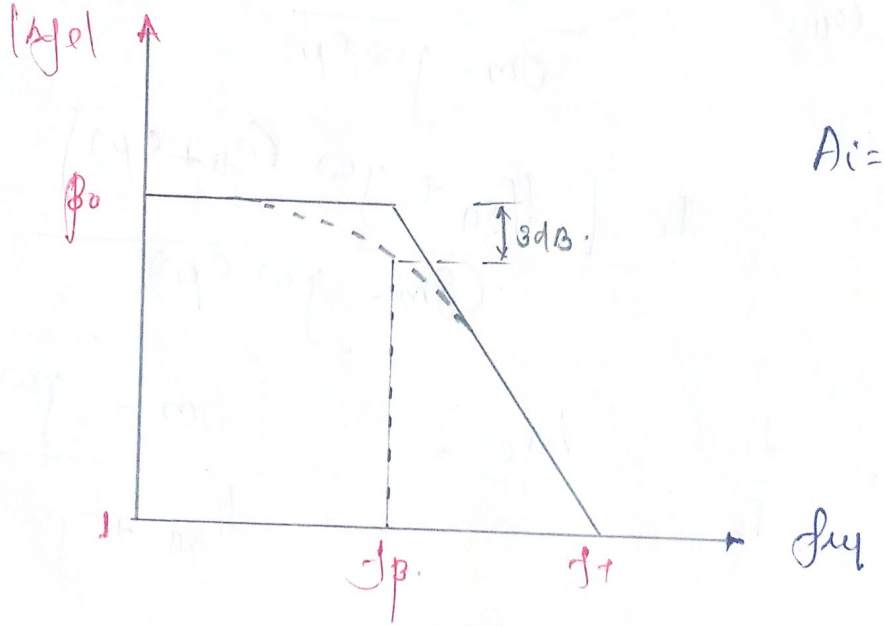
$$A_i = \frac{\beta}{1 + j\omega(C_\pi + C_\mu) r_\pi}$$

$$= \frac{1}{(C_\pi + C_\mu) r_\pi}$$

$$A_i = \frac{\beta}{1 + j \omega/\omega_\beta} = \frac{\beta}{1 + j\, \omega/\omega_\beta}$$

ω_β β cut off frequency

$$f_\beta = \frac{1}{2\pi \cdot r_\pi (C_\pi + C_\mu)}$$



$$A_i = \frac{\beta}{1 + j\, f/f_\beta}$$

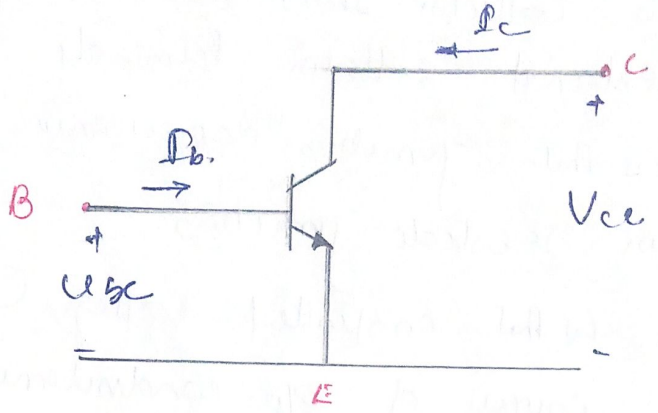
f_T is the frequency at which the short circuit current gain equal to unity (unity gain bandwidth)

$$|A_{fT}| = \frac{\beta}{\sqrt{1 + (f/f_\beta)^2}}$$

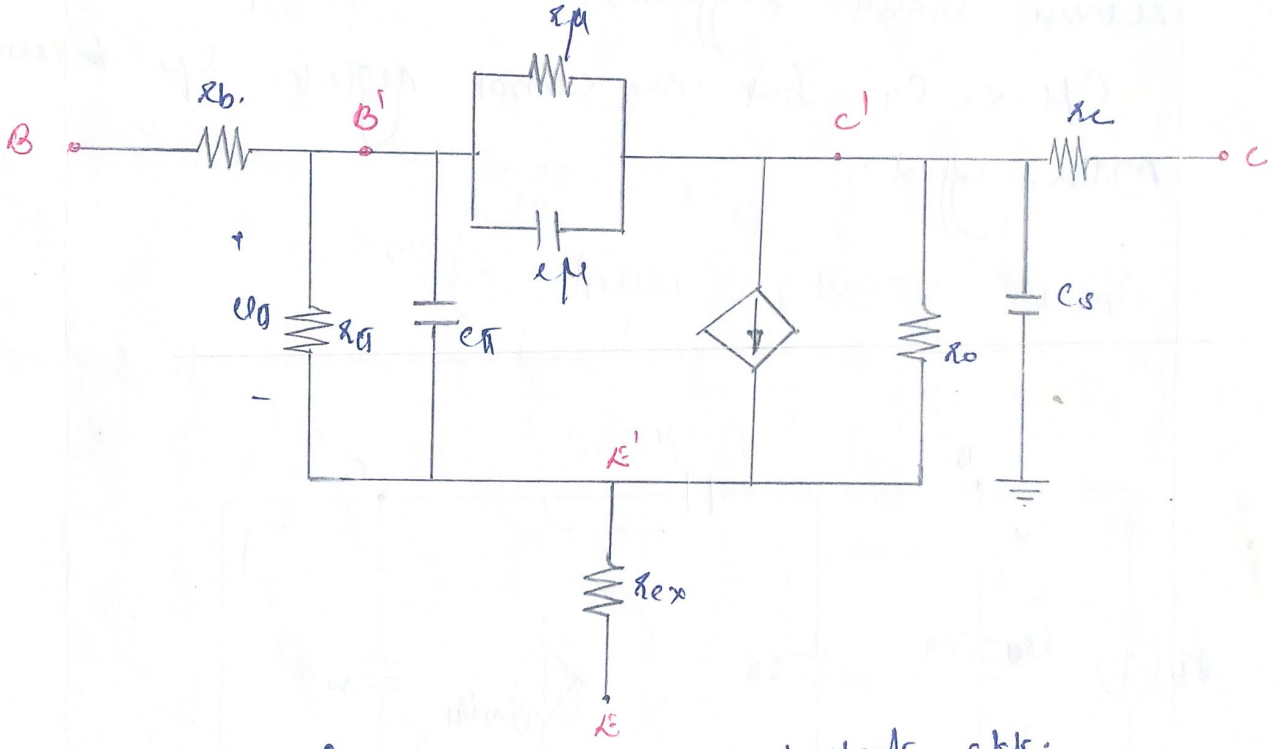
MODULE 3

CS 205

Hybrid - π Equivalent ckt [High frequency].



CE npn transistor with small signal currents and voltages.



High freq Hybrid π equivalent ckt.

rb is the base series resistance between external base terminal B and internal base region B'. B'-E' junction is forward biased. So cπ is the forward biased junction capacitance and rπ is the forward biased junction resistance.

r_{ex} is the emitter series resistance between external emitter terminal and internal emitter region.

r_c is collector series resistance between internal and external collector terminals.

C_s is the junction capacitance of reverse biased collector - substrate junction.

$g_m v_{\pi}$ is the controlled voltage source

r_o is inverse of o/p conductance g_o.

Since B'C junction is reverse biased C_μ is the junction capacitance of B'C junction. r_μ is the reverse biased diffusion resistance (r_μ is in MΩ)

$C_\mu << C_\pi$ but we cannot neglect C_μ because of Miller effect.

Short - Circuit Current Gain:

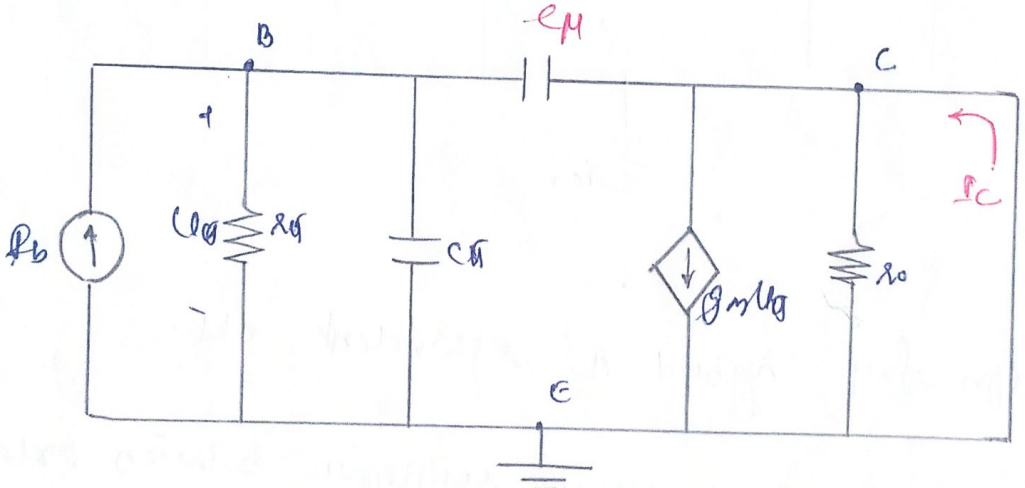


Figure shows simplified hybrid π model for transistor with neglecting r_b, r_c, r_{ex}, r_μ & C_s.

Short circuit current gain

$$A_i = \frac{I_c}{I_b}.$$

KCL at input node

$$I_b = \frac{V_\pi}{r_\pi} + \frac{V_\pi}{1/j\omega C_\pi} + \frac{V_\pi}{1/j\omega C_\mu}$$

$$I_b = V_\pi \left[1/r_\pi + j\omega (C_\pi + C_\mu) \right] \quad \text{--- (1)}$$

KCL at o/p node;

$$\frac{V_\pi}{1/j\omega C_\mu} + I_c = g_m V_\pi$$

$$I_c = V_\pi (g_m - j\omega C_\mu) \quad \text{---- (2)}$$

$$V_\pi = \frac{I_c}{g_m - j\omega C_\mu}$$ sub. in eqn (1)

$$I_b = \frac{I_c \left[1/r_\pi + j\omega (C_\pi + C_\mu) \right]}{(g_m - j\omega C_\mu)}$$

$$A_i = \frac{I_c}{I_b} = h_{fe} = \frac{g_m - j\omega C_\mu}{1/r_\pi + j\omega (C_\pi + C_\mu)}$$

$$A_i = h_{fe} \cong \frac{g_m}{1/r_\pi + j\omega (C_\pi + C_\mu)} \quad \because \omega C_\mu << g_m$$

$$\boxed{A_i = h_{fe} = \frac{g_m r_\pi}{1 + j\omega r_\pi (C_\pi + C_\mu)}}$$

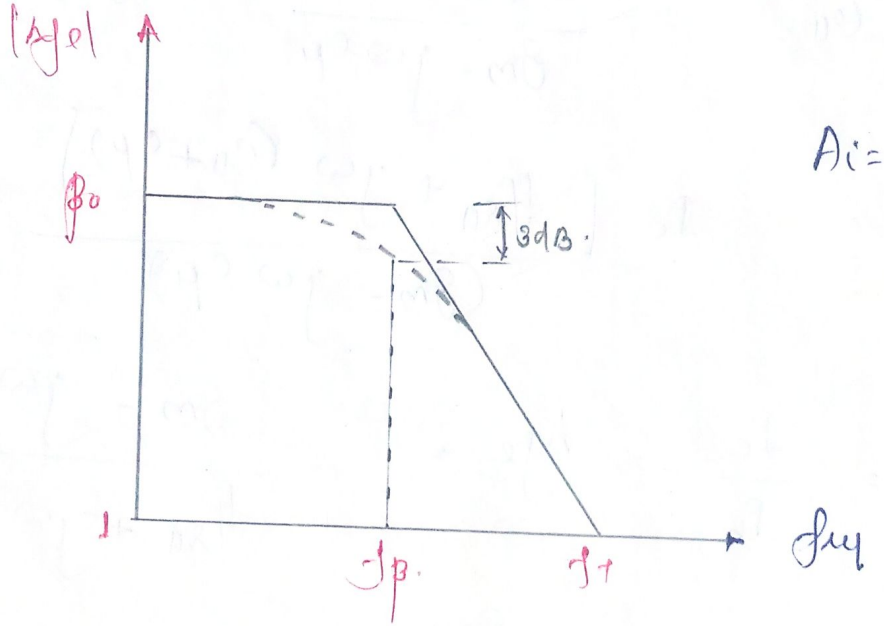
$$A_i = \frac{\beta}{1 + j\omega(C_\pi + C_\mu) r_\pi}$$

$$= \frac{1}{(C_\pi + C_\mu) r_\pi}$$

$$A_i = \frac{\beta}{1 + j \omega/\omega_\beta} = \frac{\beta}{1 + j\, \omega/\omega_\beta}$$

ω_β β cut off frequency

$$f_\beta = \frac{1}{2\pi \cdot r_\pi (C_\pi + C_\mu)}$$



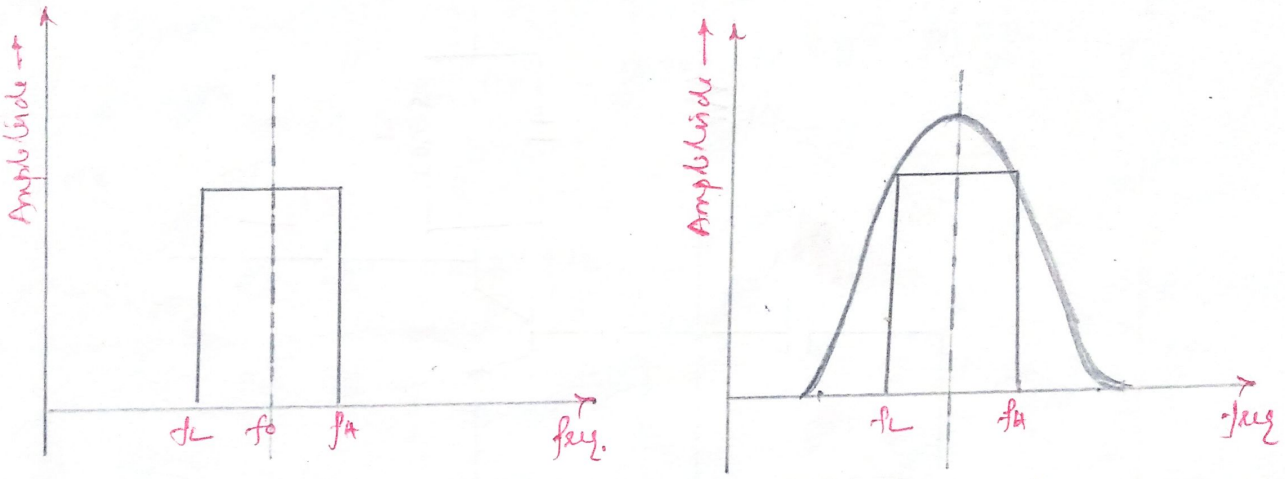
$$A_i = \frac{\beta}{1 + j\, f/f_\beta}$$

f_T is the frequency at which the short circuit current gain equal to unity (unity gain bandwidth)

$$|A_{fT}| = \frac{\beta}{\sqrt{1 + (f/f_\beta)^2}}$$

Tuned Amplifiers.

Tuned amplifiers employ a tuned ckt either at input or at o/p to make the ckt respond only to a particular range of frequencies. These amplifiers amplify signals within a narrow frequency band centered about a frequency ω_0.



Ideal & Actual frequency response of tuned amplifier

: Classification of Tuned Amplifiers:

1. Single Tuned Amplifier ⇒ Tuned either at input or at output for a particular frequency
2. Double Tuned Amplifier ⇒ Uses two tuned ckts ~~tuned~~ ~~boost~~ at input / ~~xxx~~ output for the same frequency.
3. Synchronous Tuned Amp ⇒ This is a cascade stage of single tuned amplifiers with all tuning circuits are tuned to same frequency

4. Stagger tuned Amplifier ⇒

This is also a cascade stage of tuned amplifier where the tuning circuits are tuned to slightly different frequencies to achieve a wider bandwidth.

: Single Tuned Amplifier :

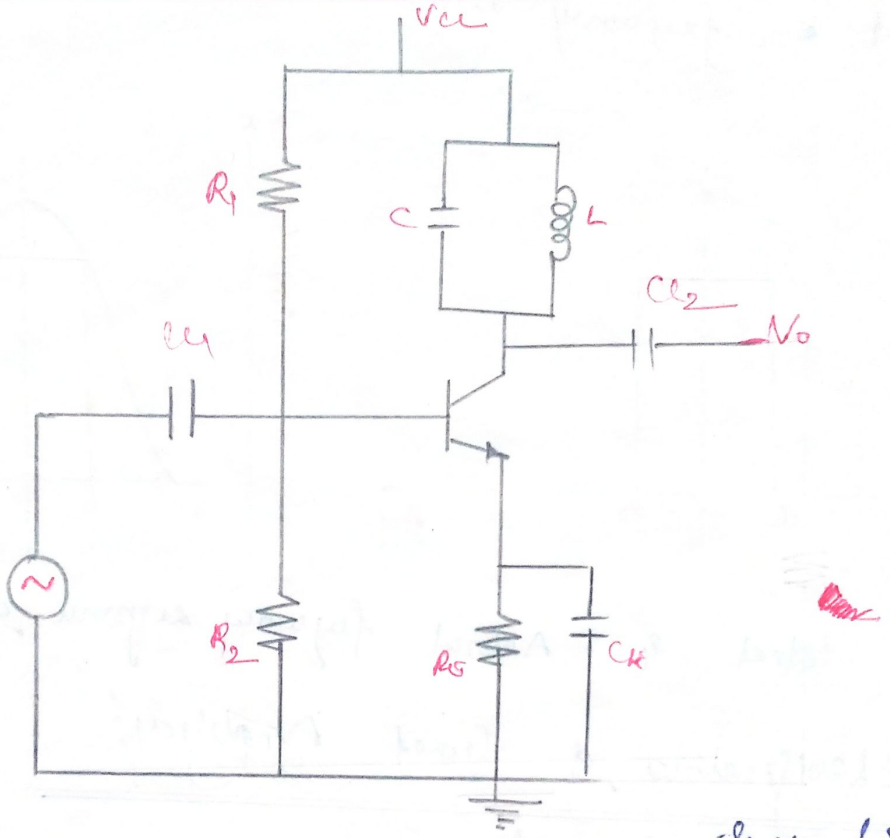
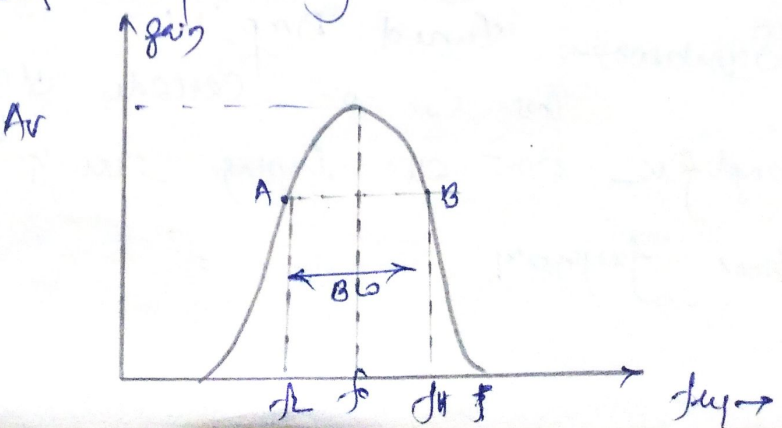


Figure is a capacitively coupled single tuned amp^r. Here the tuned ckt act as load. In this amplifier the values of capacitor (C) and inductance are selected in such a manner that the resonant frequency of tuned ckt is equal to the frequency to be selected and amplified.



BW = $f_H - f_L$ = f_0/Q

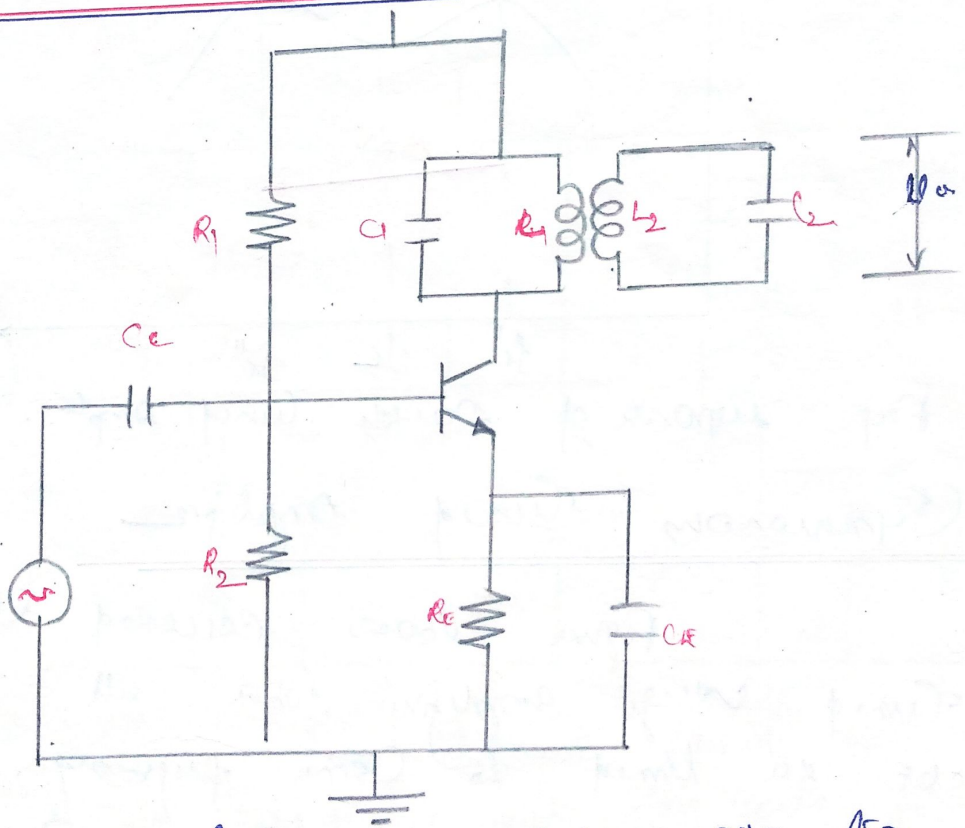
Q is the quality factor of tuned ckt.

Limitation:

Tuned amplifiers are required to be highly selective. But high selectivity requires high Q. factor. But it reduces B.W. ckt coils high Q. factor. But it reduces B.W.

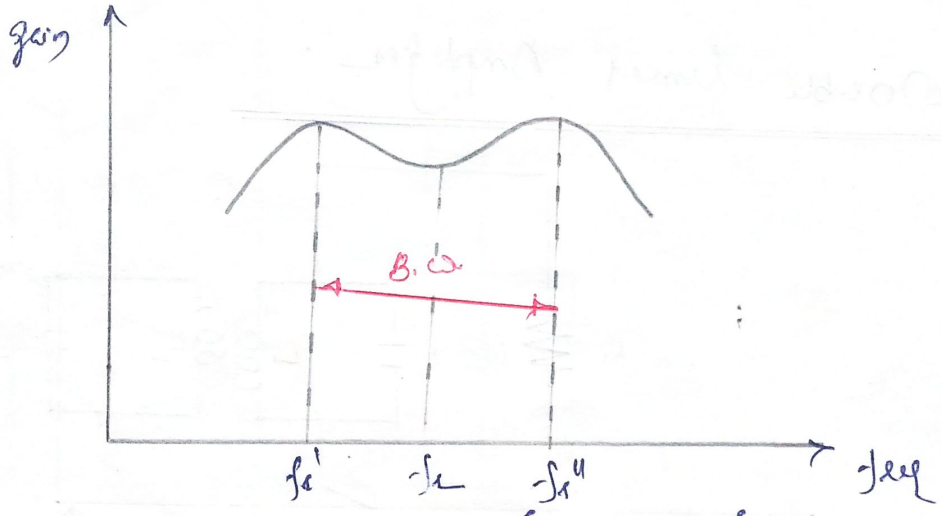
Narrow BW of amplifier causes result in poor reproduction of audio signal is the major limitation of this ckt.

Double tuned Amplifier:



It uses a transistor amplifier with two tuned circuits, one of them [L_1C_1] is shown in collector and other (L_2C_2) at load. R_1, R_2, R_E are used for biasing & stabilization

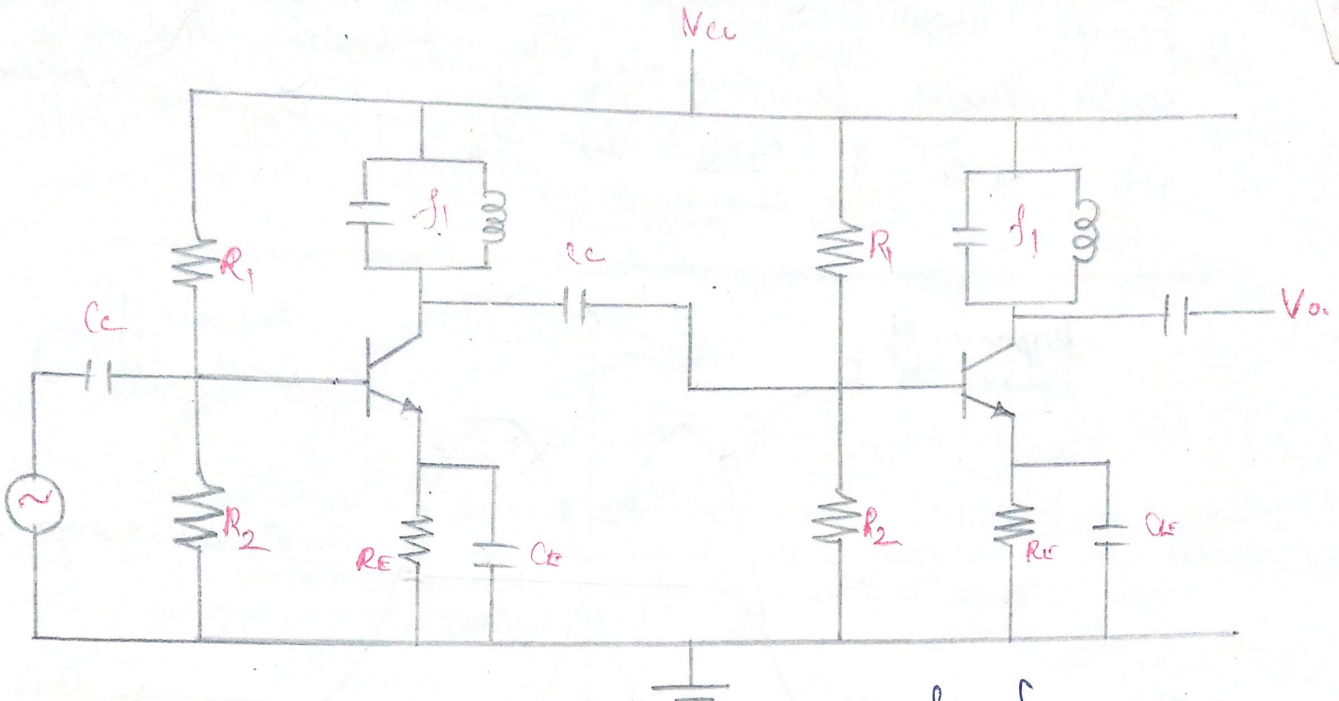
The signal to be amplified is connected to i/p tuned through cq.
The resonant frequency of resonant ckt L_1C_1 is made equal to input frequency. Under these conditions, the tuned ckt offers very high impedance & a large o/p appears across tuned ckt. The o/p from this tuned ckt is inductively coupled to L_2C_2 tuned ckt.
This type of tuned ckt is extensively used in IF amplifiers in audio & TV receivers.



Freq response of double tuned amp^r.

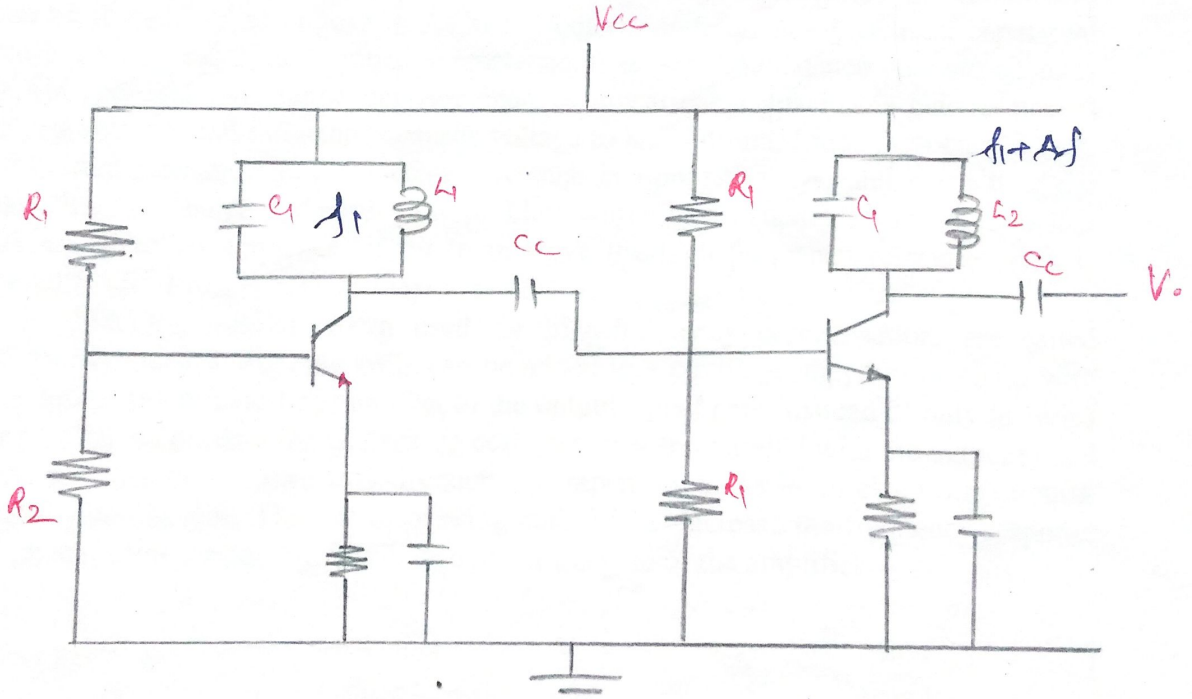
Synchronous Tuned Amplifier

Figure shows cascaded Synchronous tuned stage amplifier when all tuned ckt are tuned to same frequency.
But with Synchronous tuning Overall Bandwidth decreases.



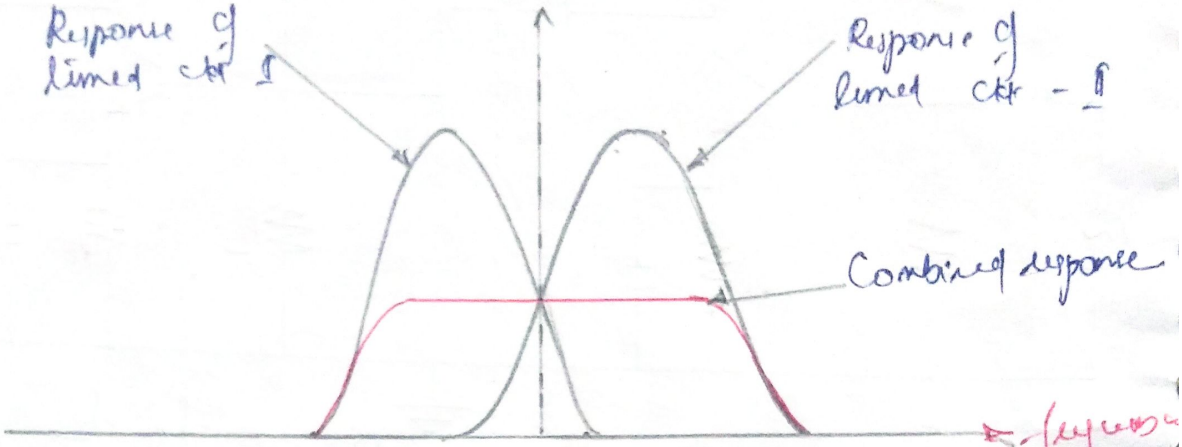
Synchronous tuning with $f_1 = f_2$

Stagger - Tuned Amplifier.



If we cascade two different tuned ckts which are tuned to slightly different frequencies, it is possible to increase the Bandwidth with flat pass band this is known as Stagger - tuning.

Figure shows a stagger tuned amplifier. Here stagger tuning is achieved by resonating the tuned ckts L_1C_1 & L_2C_2 to slightly different frequencies.



Frequency response of stagger tuned amplifier.

MODULE 4

CS 205

FEEDBACK AMPLIFIER

1 INTRODUCTION

An ideal amplifier will provide a stable output which is in an amplified version of the input signal. But the gain and stability of practical amplifiers is not very good because of device parameter variation or due to changes in ambient temperature and nonlinearity of the device. This problem can be avoided by the technique of feedback wherein a portion of the output signal is feedback to the input and combined with the input signal to produce the desired output. The feedback can be either negative (degenerative) or positive (regenerative).In negative feedback a portion of the output signal is subtracted from the input signal and in positive feedback a portion of the output signal is added to the input signal to produce desired output. Negative feedback plays a very important role in almost all the amplifier stabilization of biasing circuits, it causes the location of the quiescent point to become stable. Thus it maintain a constant value of amplifier gain against temperature variation, supply voltage etc. The feedback may be classified into two types.

1.1 Types of feedback

(i) Positive feedback. When the feedback energy (voltage or current) is in phase with the input signal and thus aids it, it is called positive feedback. This is illustrated in Fig. 1.1. Both amplifier and feedback network introduce a phase shift of 180°. The result is a 360° phase shift around the loop, causing the feedback voltage Vf to be in phase with the input signal Vin.

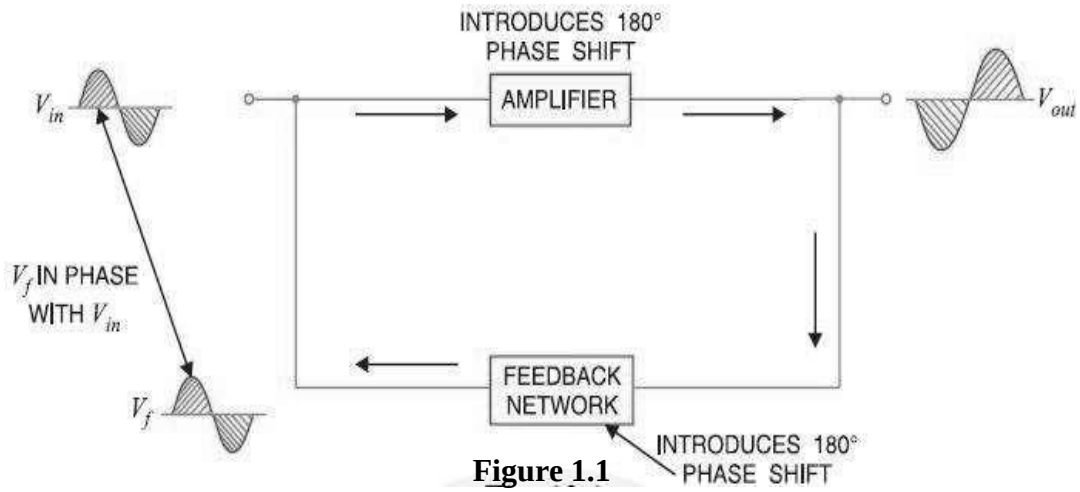


Figure 1.1

The positive feedback increases the gain of the amplifier. However, it has the disadvantages of increased distortion and instability. Therefore, positive feedback is seldom employed in amplifiers. One important use of positive feedback is in oscillators. As we shall see in the next chapter, if positive feedback is sufficiently large, it leads to oscillations. As a matter of fact, an oscillator is a device that converts d.c. power into a.c. power of any desired frequency.

(ii) Negative feedback. When the feedback energy (voltage or current) is out of phase with the input signal and thus opposes it, it is called negative feedback. This is illustrated in Fig. 1.2. As you can see, the amplifier introduces a phase shift of 180° into the circuit while the feedback network is so designed that it introduces no phase shift (i.e., 0° phase shift). The result is that the feedback voltage Vf is 180° out of phase with the input signal Vin.

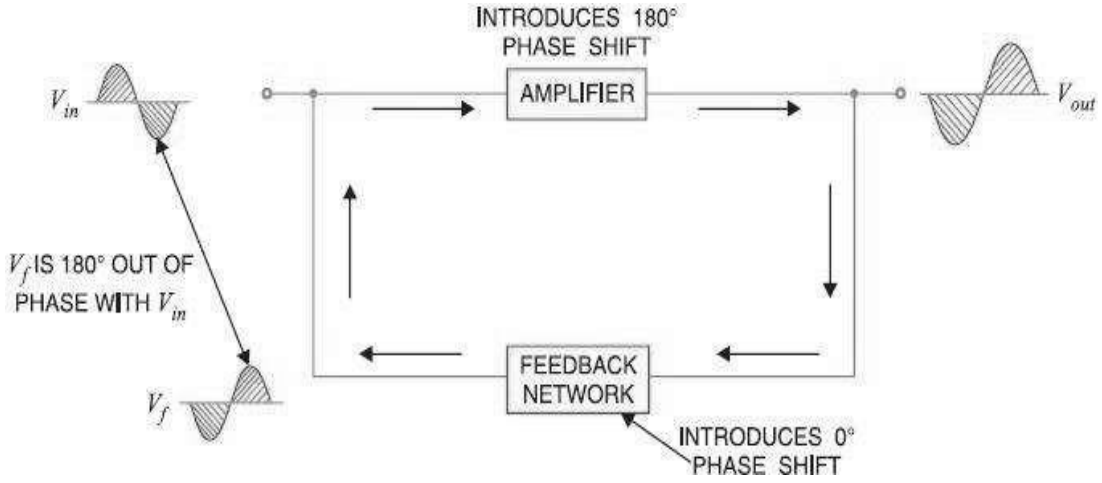


Figure 1.2

Negative feedback reduces the gain of the amplifier. However, the advantages of negative feedback are: reduction in distortion, stability in gain, increased bandwidth and improved input and output impedances. It is due to these advantages that negative feedback is frequently employed in amplifiers.

1.2 Principles of Negative Voltage Feedback in Amplifiers

A feedback amplifier has two parts viz an amplifier and a feedback circuit. The feedback circuit usually consists of resistors and returns a fraction of output energy back to the input. Fig. 1.3 *shows the principles of negative voltage feedback in an amplifier. Typical values have been assumed to make the treatment more illustrative. The output of the amplifier is 10 V. The fraction mv of this output i.e. 100 mV is fedback to the input where it is applied in series with the input signal of 101 mV. As the feedback is negative, therefore, only 1 mV appears at the input terminals of the amplifier. Referring to Fig. 1.3, we have, Gain of amplifier without feedback,

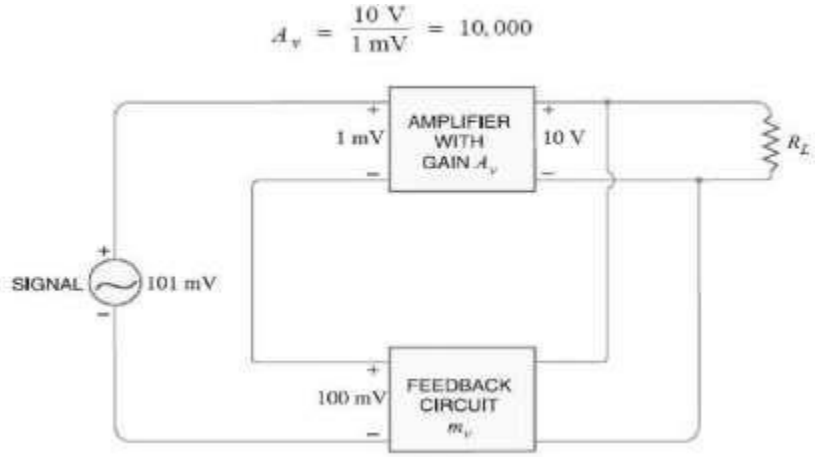


Figure 1.3

$$\text{Fraction of output voltage fedback, } m_v = \frac{100\text{ mV}}{10\text{ V}} = 0.01$$

$$\text{Gain of amplifier with negative feedback, } A_{vf} = \frac{10\text{ V}}{101\text{ mV}} = 100$$

The following points are worth noting:

- When negative voltage feedback is applied, the gain of the amplifier is reduced. Thus, the gain of above amplifier without feedback is 10,000 whereas with negative feedback, it is only 100.
- When negative voltage feedback is employed, the voltage actually applied to the amplifier is extremely small. In this case, the signal voltage is 101 mV and the negative feedback is 100 mV so that voltage applied at the input of the amplifier is only 1 mV.
- In a negative voltage feedback circuit, the feedback fraction mv is always between 0 and 1.
- The gain with feedback is sometimes called closed-loop gain while the gain without feedback is called open-loop gain. These terms come from the fact that amplifier and feedback circuits form a
  "loop". When the loop is "opened" by disconnecting the feedback circuit from the input, the amplifier's gain is Av, the "open-loop" gain. When the loop is "closed" by connecting the feedback circuit, the gain decreases to Avf , the "closed-loop" gain.

1.3 Gain of Negative Voltage Feedback Amplifier

Consider the negative voltage feedback amplifier shown in Fig. 1.4. The gain of the amplifier without Feedback is Av. Negative feedback is then applied by feeding a fraction mv

of the output voltage e0 back to amplifier input. Therefore, the actual input to the amplifier is the signal voltage e_g minus feedback voltage m_v e_0 i.e.,

Actual input to amplifier = $e_g - m_v e_0$

The output e0 must be equal to the input voltage $e_g - m_v e_0$ multiplied by gain Av of the amplifier i.e.,

$$(e_g - m_v e_0) A_v = e_0$$
$$\text{or} \quad A_v e_g - A_v m_v e_0 = e_0$$
$$\text{or} \quad e_0 (1 + A_v m_v) = A_v e_g$$
$$\text{or} \quad \frac{e_0}{e_g} = \frac{A_v}{1 + A_v m_v}$$

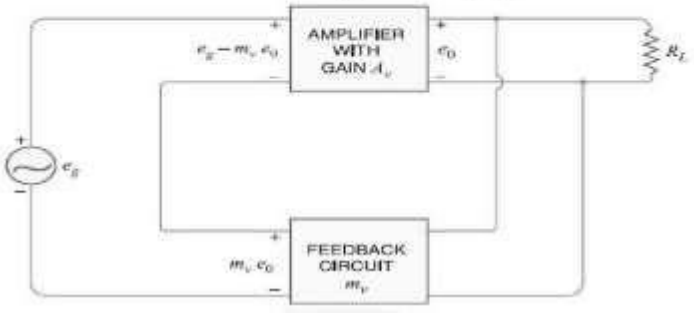


Figure 1.4

But e_0/eg is the voltage gain of the amplifier with feedback.

Voltage gain with negative feedback is

$$A_{vf} = \frac{A_v}{1 + A_v m_v}$$

It may be seen that the gain of the amplifier without feedback is Av. However, when negative voltage feedback is applied, the gain is reduced by a factor 1 + Av mv. It may be noted that negative voltage feedback does not affect the current gain of the circuit.

1.4 Advantages of Negative Voltage Feedback

The following are the advantages of negative voltage feedback in amplifiers:

(i) Gain stability. An important advantage of negative voltage feedback is that the resultant gain of the amplifier can be made independent of transistor parameters or the supply voltage variations.

$$A_{vf} = \frac{A_v}{1 + A_v\, m_v}$$

For negative voltage feedback in an amplifier to be effective, the designer deliberately makes the product Av mv much greater than unity. Therefore, in the above relation, 1 can be neglected as compared to Av mv and the expression become :

$$A_{vf} = \frac{A_v}{A_v\, m_v} = \frac{1}{m_v}$$

It may be seen that the gain now depends only upon feedback fraction mv i.e., on the characteristics of feedback circuit. As feedback circuit is usually a voltage divider (a resistive network), therefore, it is unaffected by changes in temperature, variations in transistor parameters and frequency. Hence, the gain of the amplifier is extremely stable.

(ii) Reduces distortion. A large signal stage has non-linear distortion because its voltage gain changes at various points in the cycle. The negative voltage feedback reduces the nonlinear distortion in large signal amplifiers. It can be proved mathematically that :

$$D_{vf} = \frac{D}{1 + A_v\, m_v}$$

where D = distortion in amplifier without feedback

D_{vf} = distortion in amplifier with negative feedback

It is clear that by applying negative voltage feedback to an amplifier, distortion is reduced by a factor 1 + Av mv.

(iii) Improves frequency response. As feedback is usually obtained through a resistive network, therefore, voltage gain of the amplifier is *independent of signal frequency. The result is that voltage gain of the amplifier will be substantially constant over a wide range of signal frequency. The negative voltage feedback, therefore, improves the frequency response of the amplifier.

(iv) Increases circuit stability. The output of an ordinary amplifier is easily changed due to variations in ambient temperature, frequency and signal amplitude. This changes the gain of the amplifier, resulting in distortion. However, by applying negative voltage feedback, voltage gain of the amplifier is stabilised or accurately fixed in value. This can be easily explained. Suppose the output of a negative voltage feedback amplifier has increased because of temperature change or due to some other reason. This means more negative feedback since feedback is being given from the output. This tends to oppose the increase in amplification and maintains it stable. The same is true should the output voltage decrease. Consequently, the circuit stability is considerably increased.

(v) Increases input impedance and decreases output impedance. The negative voltage feedback increases the input impedance and decreases the output impedance of amplifier. Such a change is profitable in practice as the amplifier can then serve the purpose of impedance matching.

a) Input impedance. The increase in input impedance with negative voltage feedback can be explained by referring to Fig. 1.4. Suppose the input impedance of the amplifier is Z_{in} without feedback and Z ′in with negative feedback. Let us further assume that input current is i1. Referring to Fig. 1.5, we have,

$$e_g - m_v e_0 = i_1 Z_{in}$$

Now

$$\begin{aligned} e_g &= (e_g - m_v e_0) + m_v e_0 \\ &= (e_g - m_v e_0) + A_v m_v (e_g - m_v e_0) \qquad [\because e_0 = A_v (e_g - m_v e_0)] \\ &= (e_g - m_v e_0)(1 + A_v m_v) \\ &= i_1 Z_{in} (1 + A_v m_v) \qquad [\because e_g - m_v e_0 = i_1 Z_{in}] \end{aligned}$$

or

$$\frac{e_g}{i_1} = Z_{in} (1 + A_v m_v)$$

But eg/i1 = Z ′i n , the input impedance of the amplifier with negative voltage feedback.

$$Z'_{in} = Z_{in} (1 + A_v m_v)$$

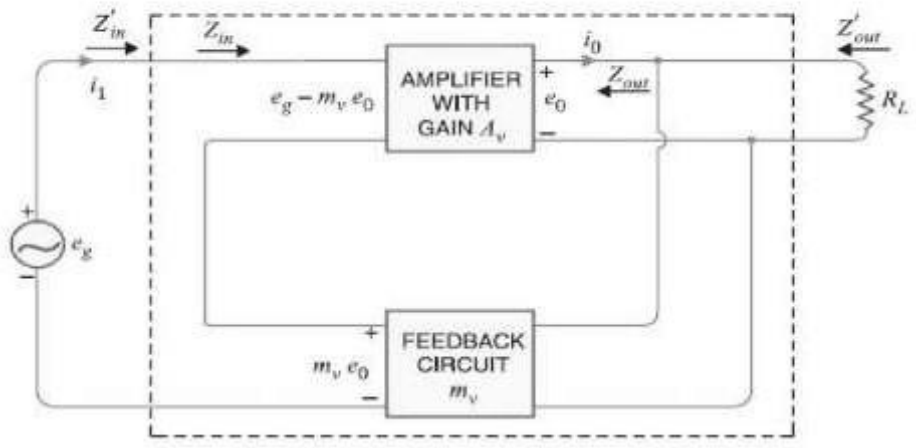


Figure 1.5

It is clear that by applying negative voltage feedback, the input impedance of the

amplifier is increased by a factor 1 + Aν mv. As Aν mv is much greater than unity, therefore, input impedance is increased considerably. This is an advantage, since the amplifier will now present less of a load to its source circuit.

(b) Output impedance. Following similar line, we can show that output impedance with negative voltage feedback is given by

$$Z'_{out} = \frac{Z_{out}}{1 + A_v\, m_v}$$

where Z'_{out} = output impedance with negative voltage feedback

Z_{out} = output impedance without feedback

It is clear that by applying negative feedback, the output impedance of the amplifier is decreased by a factor 1 + Aν mv. This is an added benefit of using negative voltage feedback. With lower value of output impedance, the amplifier is much better suited to drive low impedance loads.

Disadvantages of negative feedback amplifier

- Reduced circuit overall gain
- Reduced stability at high frequency

1.5 Feedback Circuit

The function of the feedback circuit is to return a fraction of the output voltage to the input of the amplifier. Fig. 1.6 shows the feedback circuit of negative voltage feedback amplifier. It is essentially a potential divider consisting of resistances R1 and R2. The output voltage of the amplifier is fed to this potential divider which gives the feedback voltage to the input. Referring to Fig. 1.6, it is clear that:

$$\text{Voltage across } R_1 = \left(\frac{R_1}{R_1 + R_2}\right) e_0$$

$$\text{Feedback fraction, } m_v = \frac{\text{Voltage across } R_1}{e_0} = \frac{R_1}{R_1 + R_2}$$

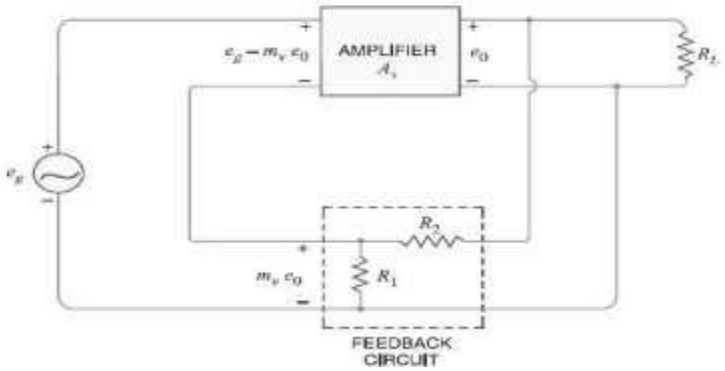


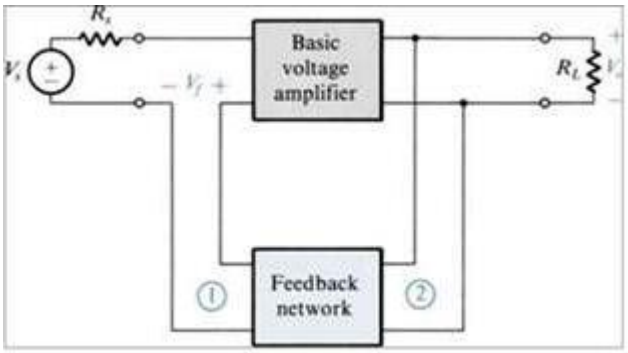
Figure 1.6

1.6 Basic Feedback Topologies

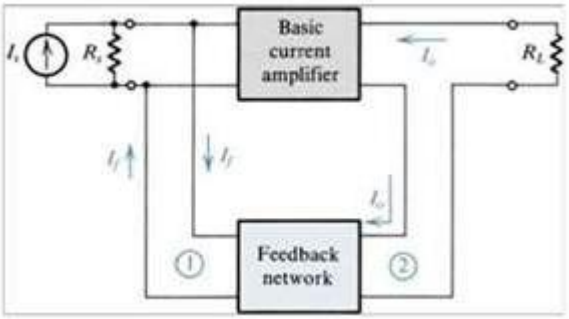
Depending on the input signal (voltage or current) to be amplified and form of the output (voltage or current), amplifiers can be classified into four categories. Depending on the amplifier category, one of four types of feedback structures should be used.

Voltage series feedback (*Af = Vo/Vs)* – Voltage amplifier
Voltage shunt feedback (*Af = Vo/Is)* – Trans-resistance amplifier
Current series feedback (*Af = Io /Vs)* - Trans-conductance amplifier
Current shunt feedback (*Af = Io/Is)* - Current amplifier

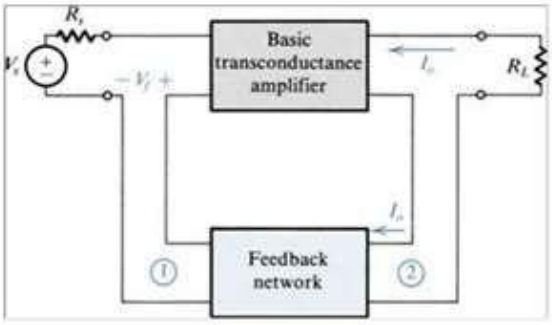
Here voltage refers to connecting the output voltage as input to the feedback network. Similarly current refers to connecting the output current as input to the feedback network. Series refers to connecting the feedback signal in series with the input voltage; Shunt refers to connecting the feedback signal in shunt (parallel) with an input current source.



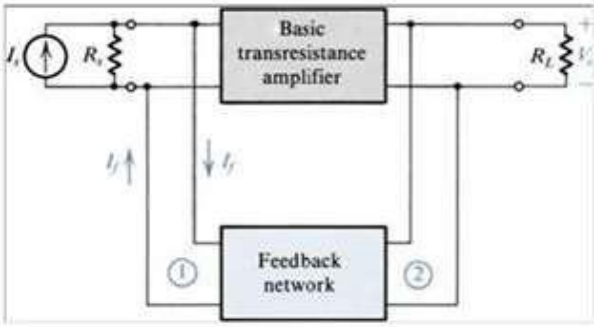
(a)



(b)



(c)



(d)

The four basic feedback topologies: (a) voltage-sampling series-mixing (series-shunt) topology, (b) current-sampling shunt-mixing (shunt-series) topology, (c) current-sampling series-mixing (series-series) topology, (d) voltage-sampling shunt-mixing (shunt-shunt) topology.

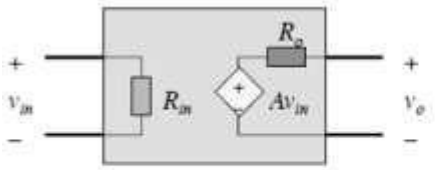
Table Effects of Feedback[a]

Feedback Type	x_s	x_o	Gain Stabilized	Input Impedance	Output Impedance	Ideal Amplifier
Series voltage	v_s	v_o	$A_{vf} = \frac{A_v}{1 + A_v\beta}$	$R_i(1 + A_v\beta)$	$\frac{R_o}{1 + \beta A_{voc}}$	Voltage
Series current	v_s	i_o	$G_{mf} = \frac{G_m}{1 + G_m\beta}$	$R_i(1 + G_m\beta)$	$R_o(1 + \beta G_{msc})$	Transconductance
Parallel voltage	i_s	v_o	$R_{mf} = \frac{R_m}{1 + R_m\beta}$	$\frac{R_i}{1 + R_m\beta}$	$\frac{R_o}{1 + \beta R_{moc}}$	Transresistance
Parallel current	i_s	i_o	$A_{if} = \frac{A_i}{1 + A_i\beta}$	$\frac{R_i}{1 + A_i\beta}$	$R_o(1 + \beta A_{isc})$	Current

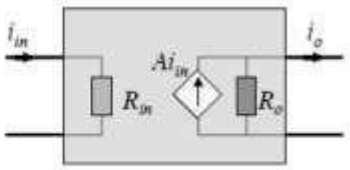
[a] Formulas given assume an ideal controlled source for the feedback network (as shown in Figure 9.14), zero source impedance for series feedback, and infinite source impedance for parallel feedback. Gains with subscripts sc and oc are for short-circuit and open-circuit loads, respectively. The gains A_v, G_m, R_m, and A_i are for the actual load.

1.6 Types of Negative Feedback Connection

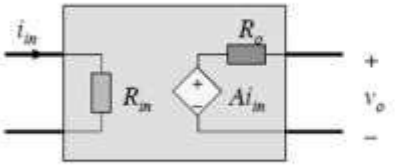
Models of Amplifier



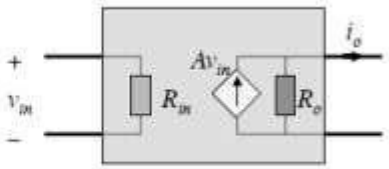
voltage amplifier



current amplifier



transresistance amplifier



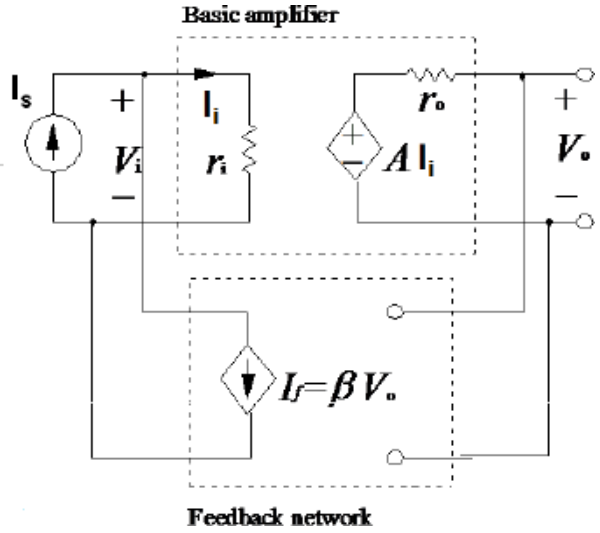
transconductance amplifier

1.7. Feedback topologies

Voltage shunt feedback

Voltage gain

$$V_o = A \cdot I_i = A(I_S - I_f)$$
$$I_f = \beta \cdot V_o$$
$$A(I_S - \beta V_o) = V_o$$
$$AI_S = (1+\beta A)V_o$$
$$A_f = \frac{V_o}{I_S} = (\frac{A}{1+\beta A})$$



Input impedance

$$Z_{\text{in}} = \frac{V_i}{I_S} = \frac{V_i}{I_i + I_f}$$
$$= \frac{I_i \cdot r_i}{I_i + \beta V_o)} = \frac{I_i \cdot r_i}{I_i + \beta A I_i}$$
$$Z_{\text{in}} = \frac{r_i}{(1+\beta A)}$$

Output impedance

$$Z_{\text{out}}\,|_{V_S=0} = \frac{V_o}{I_o}$$

from input port,

$$I_i = -I_f = -\beta V_o$$

from output port,

$$I_o = \frac{V_o - AI_i}{r_o} = \frac{V_o + \beta A V_o}{r_o}$$

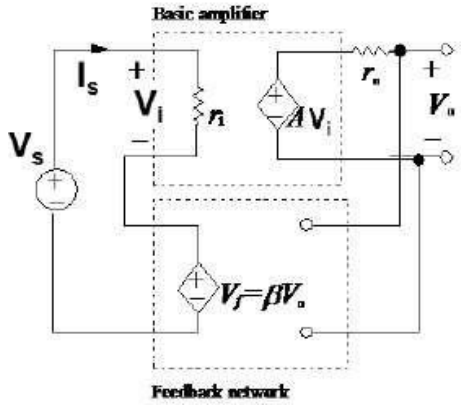
$$Z_{\text{out}} = \frac{V_o}{I_o} = \frac{r_o}{(1+\beta A)}$$

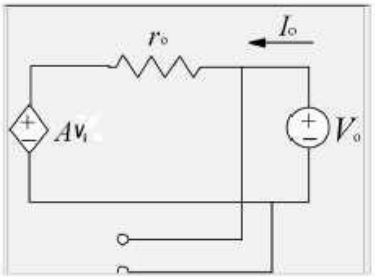
Voltage series feedback

$$V_o = A \cdot V_i = A(V_S - V_f)$$
$$V_f = \beta \cdot V_o$$
$$A(V_S - \beta V_o) = V_o$$
$$AV_S = (1+\beta A)V_o$$
$$A_f = \frac{V_o}{V_S} = (\frac{A}{1+\beta A})$$

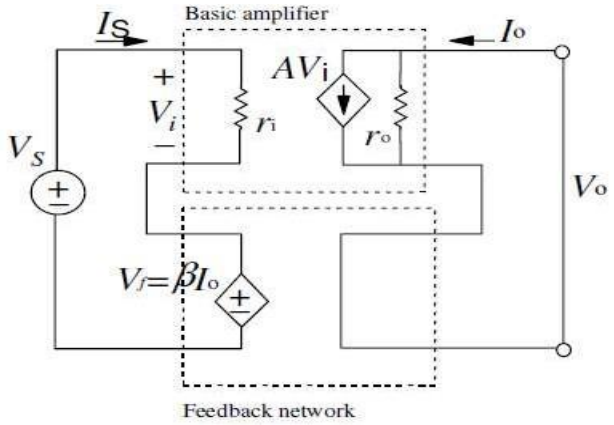
$$Z_{in} = \frac{V_S}{I_S} = \frac{V_i + V_f}{I_S}$$
$$= \frac{V_i + \beta V_o}{I_S} = \frac{V_i + \beta A V_i}{I_S}$$
$$Z_{in} = \frac{V_i(1+\beta A)}{I_S} = r_i(1+\beta A)$$

$$Z_{out}\,|_{V_S=0} = \frac{V_o}{I_o}$$
$$I_o = \frac{V_o - A \cdot V_i}{r_o}$$
$$V_i + \beta \cdot V_o = V_S = 0$$
$$V_i = -\beta \cdot V_o$$
$$I_o = \frac{V_o + A \cdot \beta \cdot V_o}{r_o}$$
$$Z_{out} = \frac{V_o}{I_o} = \frac{r_o}{1 + A \cdot \beta}$$





Current series feedback



Voltage Gain

$$I_o = A \cdot V_i = A(V_S - V_f)$$
$$V_f = \beta \cdot I_o$$
$$A(V_S - \beta I_o) = I_o$$
$$AV_S = (1+\beta A)I_o$$
$$A_f = \frac{I_o}{V_S} = (\frac{A}{1+\beta A})$$

Input Impedance

$$Z_{\text{in}} = \frac{V_S}{I_S} = \frac{V_i + V_f}{I_S}$$
$$= \frac{V_i + \beta V_o}{I_S} = \frac{V_i + \beta A V_i}{I_S}$$
$$Z_{\text{in}} = \frac{V_i(1+\beta A)}{I_S} = r_i(1+\beta A)$$

Output Impedance

$$V_i + V_f = V_S = 0 \qquad Z_{\text{out}}|_{V_S=0} = \frac{V_o}{I_o}; I_o = \frac{V_o - A \cdot V_i}{r_o}$$

$$I_o = \frac{V_o + A \cdot \beta \cdot I_o}{r_o} \qquad \boxed{Z_{\text{out}} = \frac{V_o}{I_o} = \frac{r_o}{1 + A \cdot \beta}}$$

1.8 Analysis of Emitter Follower

It is a negative current feedback circuit. The emitter follower is a current amplifier that has no voltage gain. Its most important characteristic is that it has high input impedance and low output impedance. This makes it an ideal circuit for impedance matching.

1.8.1 Circuit details. Fig.1.8 shows the circuit of an emitter follower. As you can see, it differs from the circuitry of a conventional CE amplifier by the absence of collector load and emitter bypass capacitor. The emitter resistance RE itself acts as the load and a.c. output voltage (Vout) is taken across RE. The biasing is generally provided by voltage-divider method or by base resistor method. The following points are worth noting about the emitter follower :

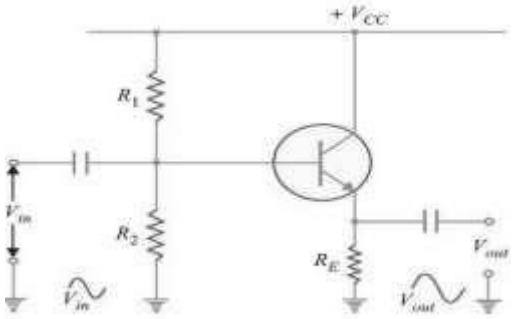


Figure. 1.8

Oscillators

4.1 General Concepts:

An ***oscillator*** is a device that generates a periodic ac output signal without any form of input signal required with only the dc supply voltage as an input. The output voltage can be either ***sinusoidal*** or ***nonsinusoidal*** (see Fig. 4-1). Two major classifications of oscillators are ***feedback*** oscillators and ***relaxation*** oscillators; an oscillator is designed to have a feedback path with known characteristics, so that a predictable oscillation will occur at a predetermined frequency.

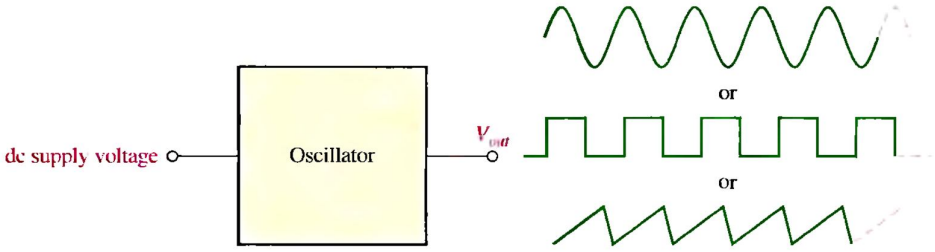


Fig. 4-1

One type of oscillator is the feedback oscillator, which returns a fraction of the output signal to the input with no net phase shift, resulting in a reinforcement of the output signal. After oscillations are started, the loop gain is maintained at 1 to maintain oscillations. A feedback oscillator consists of an amplifier for gain (either a discrete transistor or an op-amp) and a positive feedback circuit that produces phase shift and provides attenuation, as shown in Fig. 4-2.

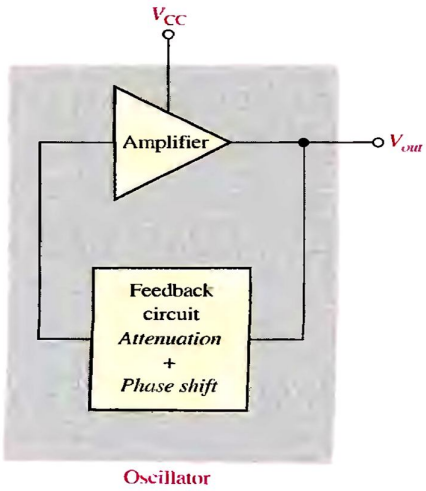


Fig. 4-2

A second type is a relaxation oscillator uses an *RC* timing circuit to generate a waveform that is generally a square wave or other nonsinusoidal waveform. Typically, a relaxation oscillator uses a Schmitt trigger or other device that changes states to alternately charge and discharge a capacitor through a resistor.

4.2 Feedback Oscillators:

Feedback oscillator operation is based on the principle of positive feedback. Feedback oscillators are widely used to generate sinusoidal waveforms. Positive feedback is characterized by the condition wherein an in-phase portion of the output voltage of an amplifier is fed back to the input with no net phase shift, resulting in a reinforcement of the output signal. As shown in Fig. 4-3, the in-phase feedback voltage, V_f is amplified to produce the output voltage, which in turn produces the feedback voltage. That is, a loop is created in which the signal sustains itself and a continuous sinusoidal output is produced. This phenomenon is called ***oscillation***.

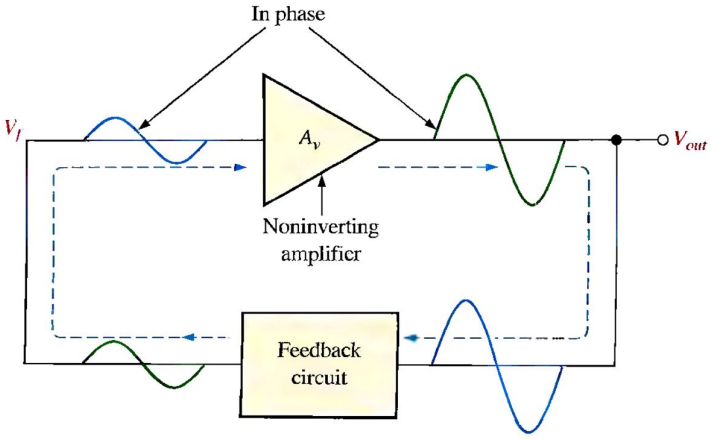


Fig. 4-3

Two conditions, illustrated in Fig. 4-4, are required for a sustained state of oscillation:

1. The phase shift around the feedback loop must be effectively 0°.

2. The voltage gain, A, around the closed feedback loop (loop gain) must equal 1 (unity).

The unity-gain condition must be met for oscillation to be sustained. For oscillation to begin, the voltage gain around the positive feedback loop must be greater than 1 so that the amplitude of the output can build up to a desired level. The gain must then decrease to 1 so that the output stays at the desired level and oscillation is sustained.

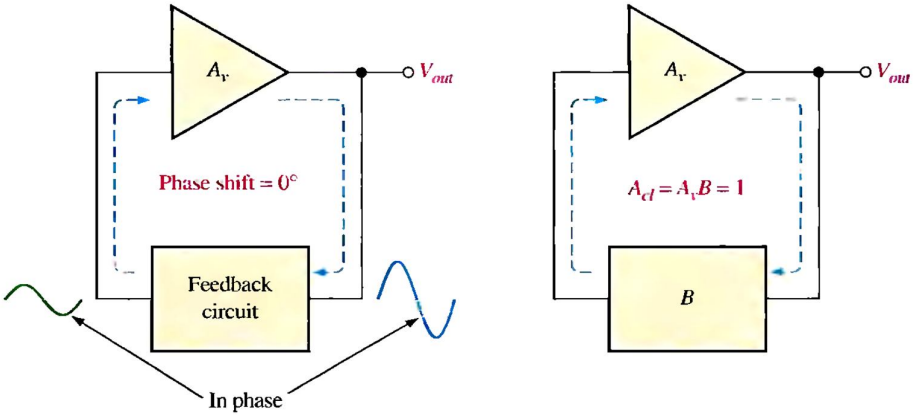


Fig. 4-4

A question that normally arises is this: If the oscillator is initially off and there is no output voltage. How does a feedback signal originate to start the positive feedback buildup process? Initially a small positive feedback voltage develops from thermally produced broad-band noise in the resistors or other components or from power supply turn-on transients. The feedback circuit permits only a voltage with a frequency equal to the selected oscillation frequency to appear in phase on the amplifier's input. This initial feedback voltage is amplified and continually reinforced, resulting in a buildup of the output voltage, as illustrated in Fig. 4-5.

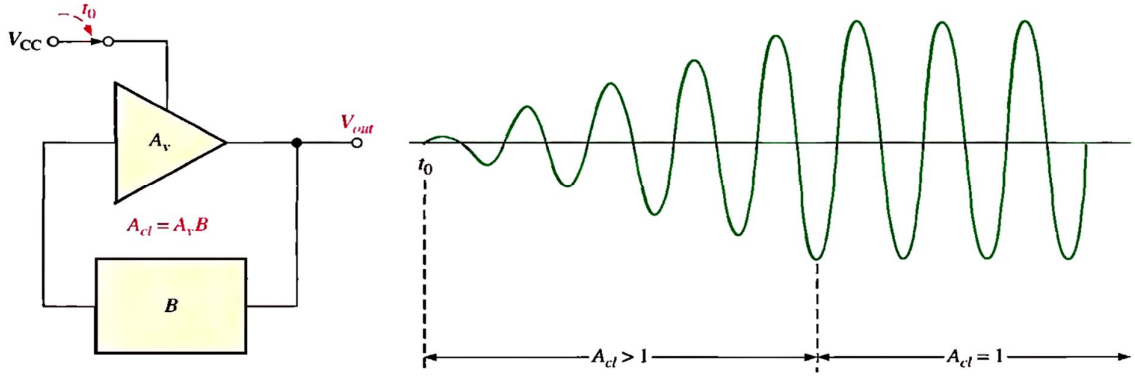


Fig. 4-5

Finally, what we mean by "feedback" feedback to where? In reality, it makes no difference where, because we have a closed loop with no summing junction at which any external input is added (see Fig. 4-5). Thus, we could start anywhere in the loop and call that point both the "input" and the "output"; we could think of the "feedback" path as the entire path through which signal flows in going completely around the loop of an amplifier having gain A and a feedback path having gain B. Every oscillator must have an amplifier, or equivalent device, in order for the system oscillate, the loop gain AB must satisfy the ***Barkhausen criterion***, namely, $AB = 1$. The unity loop-gain criterion for oscillation is often called positive feedback. To understand and apply the Barkhausen criterion, we must regard both the gain and the phase shift of AB as functions of frequency. To show the dependence of the loop gain AB on frequency, we write $AB(j\omega)$, a complex phasor that can be expressed in both polar and rectangular form:

$$AB(j\omega) = |AB|\angle\theta = |AB|cos\,\theta + j|AB|\sin\theta$$

where $|AB|$ is the gain magnitude, a function of frequency, and θ is the phase shift, also a function of frequency. The Barkhausen criterion requires that:

$$|AB| = 1 \quad \text{and} \quad \theta = \pm 360°n$$

where n is any integer, including 0. In polar and rectangular forms, the Barkhausen criterion is expressed as:

$$AB(j\omega) = 1\angle \pm 360°n = 1 + j0$$

4.3 Oscillators with RC Feedback Circuits:

In this section, we will study two types of feedback oscillators that use RC circuits to produce sinusoidal outputs: the Wien-bridge oscillator and the phase-shift oscillator. Generally, RC feedback oscillators are used for frequencies up to about 1 MHz.

4.3.1 Wien-Bridge Oscillators:

One type of sinusoidal feedback oscillator is the ***Wien-bridge*** oscillator. A fundamental part of the Wien-bridge oscillator is a lead-lag circuit like that shown in Fig. 4-6(a). R_1 and C_1 together form the lag portion (LPF) of the circuit; R_2 and C_2 form the lead portion (HPF). The operation of this lead-lag (BPF) circuit is as follows. At lower frequencies, the lead circuit dominates due to the high reactance of C_2. As the frequency increases, X_{C2} decreases, thus allowing the output voltage to increase. At some specified frequency, the response of the lag circuit takes over, and the decreasing value of X_{C1} causes the output voltage to decrease.

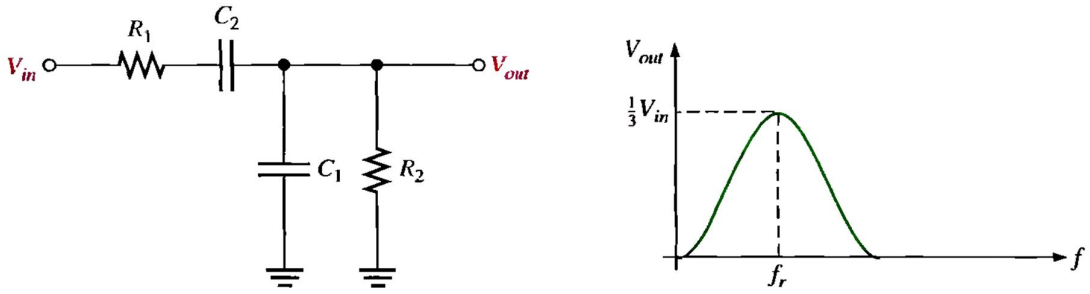
The response curve for the lead-lag circuit shown in Fig. 4-6(b) indicates that the output voltage peaks at a frequency called the resonant frequency, f_r. At this point the attenuation (V_{out}/V_{in}) of the circuit is 1/3 if $R_1 = R_2 = R$ and $C_1 = C_2 = C$ as stated by the following equation:

$$B = \frac{V_{out}}{V_{in}} = \frac{1}{3} \qquad [4\text{-}1]$$

The formula for the resonant frequency is

$$f_r = \frac{1}{2\pi RC} \qquad [4\text{-}2]$$

To summarize, the lead-lag circuit in the Wien-bridge oscillator has a resonant frequency, f_r, at which the phase shift through the circuit is 0° and the attenuation is 1/3. Below f_r, the lead circuit dominates and the output leads the input. Above f_r, the lag circuit dominates and the output lags the input.



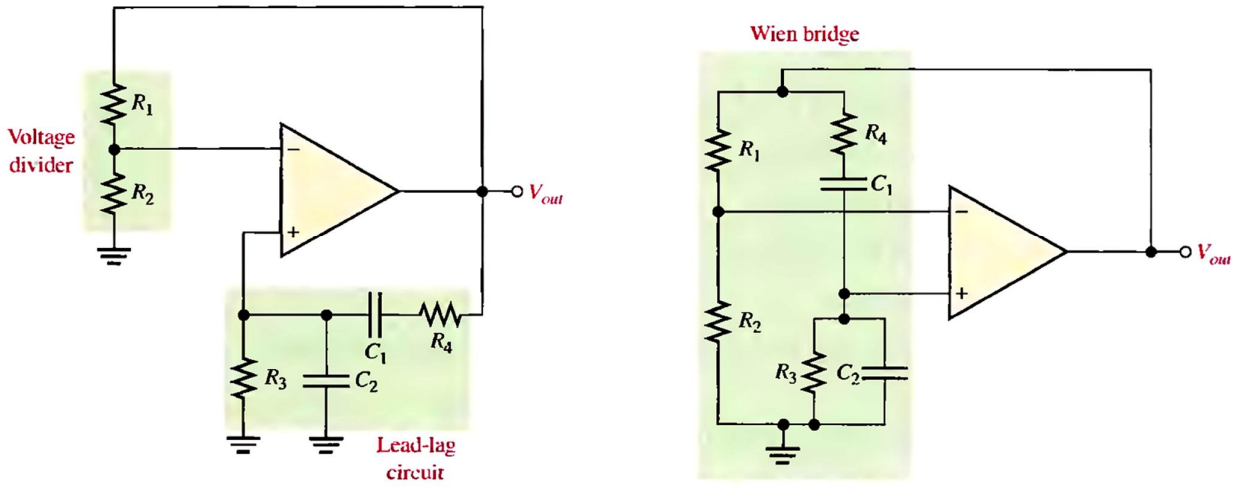
(a) (b)

Fig. 4-6

The lead-lag circuit is used in the positive feedback loop of an op-amp, as shown in Fig. 4-7(a). A voltage divider is used in the negative feedback loop. The Wien-bridge oscillator circuit can be viewed as a noninverting amplifier configuration with the input signal fed back from the output through the lead-lag circuit. Recall that the closed-loop gain of the amplifier is determined by the voltage divider.

$$A = 1 + \frac{R_1}{R_2}$$

The circuit is redrawn in Fig. 4-7(b) to show that the op-amp is connected across the bridge circuit. One leg of the bridge is the lead-lag circuit, and the other is the voltage divider.



(a) (b)

Fig. 4-7

The unity-gain condition in the feedback loop is met when

$$A = \frac{1}{B} = \frac{1}{1/3} = 3$$

This offsets the 1/3 attenuation of the lead-lag circuit, thus making the total gain around the positive feedback loop equal to 1. To achieve a closed-loop gain of 3,

$$R_1 = 2R_2$$

Then

$$A = 1 + \frac{R_1}{R_2} = 1 + \frac{2R_2}{R_2} = 3$$

The circuit in Fig. 4-8 illustrates a method for achieving sustained oscillations. Notice that the voltage-divider circuit has been modified to include an additional resistor R_3 in parallel with a back-to-back zener diode arrangement. When dc power is first applied, both zener diodes appear as opens. This places R_3 in series with R_1, thus increasing the closed-loop gain of the amplifier as follows ($R_1 = 2R_2$):

$$A = 1 + \frac{R_1+R_3}{R_2} = 1 + \frac{2R_2+R_3}{R_2} = 3 + \frac{R_3}{R_2}$$

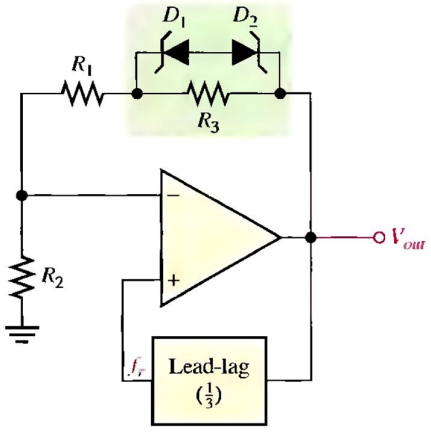


Fig. 4-8

Another method to control the gain uses a JFET as a voltage-controlled resistor in a negative feedback path. This method can produce an excellent sinusoidal waveform that is stable. A JFET operating with a small or zero V_{DS} is operating in the ohmic region. As the gate voltage increases, the drain-source resistance increases. If the JFET is placed in the negative feedback path, automatic gain control (AGC) can be achieved because of this voltage controlled resistance.

A JFET stabilized Wien bridge is shown in Fig. 4-9. The gain of the op-amp is controlled by the components shown in the dark box, which include the JFET. The JFET's drain-source resistance depends on the gate voltage. With no output signal, the gate is at zero volts, causing the drain-source resistance to be at the minimum. With this condition, the loop gain is greater than 1. Oscillations begin and rapidly build to a large output signal. Negative excursions of the output signal forward-bias D_1, causing capacitor C_3 to charge to a negative voltage. This voltage increases the drain-source resistance of the JFET and reduces the gain (and hence the output). This is classic negative feedback at work. With the proper selection of components, the gain can be stabilized at the required level.

As mentioned previously, the closed-loop gain must be 3 for oscillations to be sustained. For an inverting amplifier, the gain is that of a noninverting amplifier.

$$A = \frac{1}{B} = 1 + \frac{R_f}{R_i}$$

Referring to Fig. 4-8, R_i is composed of R_3 (the source resistor) and r'_{ds}. Substituting,

$$A = 1 + \frac{R_f}{R_3 + r'_{ds}}$$

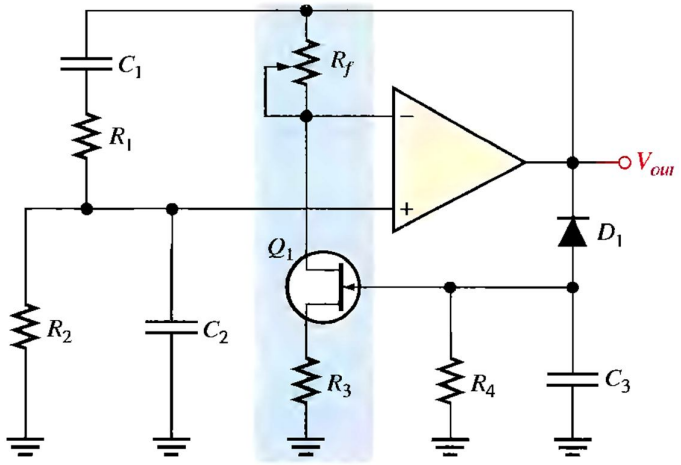


Fig. 4-9

Exercise 4-1:

(a) Determine the resonant frequency for the Wien-bridge oscillator in Fig. 4-9. Use $R_1 = R_2 = R = 10$ kΩ, $C_1 = C_2 = C = 0.01$ μF, and $R_3 = 1$ kΩ.

(b) Calculate the setting for R_f assuming the internal drain-source resistance, r'_{ds}, of the JFET is 500 Ω when oscillations are stable.

[Answers: (a) 1.59 kHz, (b) 3 kΩ]

4.3.2 Phase-Shift Oscillators:

Fig. 4-10 shows a sinusoidal feedback oscillator called the ***phase-shift*** oscillator. Each of the three RC circuits in the feedback loop can provide a maximum phase shift approaching 90°. Oscillation occurs at the frequency where the total phase shift through the three RC circuits is 180°. The inversion of the op-amp itself provides the additional 180° to meet the requirement for oscillation of a 360° (or 0°) phase shift around the feedback loop.

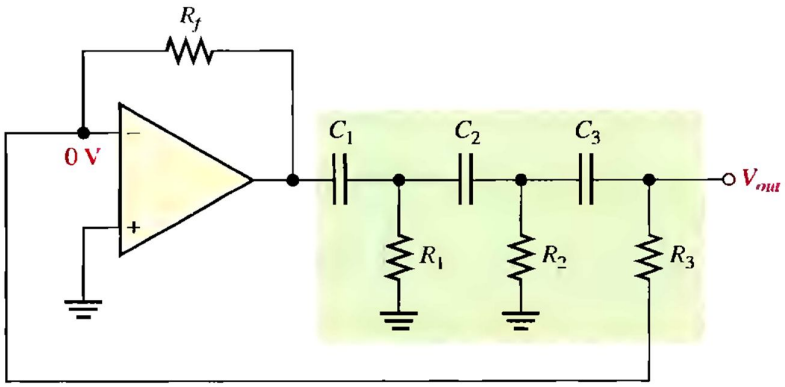


Fig. 4-10

The attenuation, B, of the three-section RC feedback circuit is:

$$B = \frac{1}{29} \qquad [4\text{-}3]$$

where $B = 1/A = R_3/R_f$

To meet the greater-than-unity loop gain requirement, the closed-loop voltage gain of the op-amp must be greater than 29 (set by R_f and R_3). The frequency of oscillation (f_r) is stated in the following equation:

$$f_r = \frac{1}{2\sqrt{6}\pi RC} \qquad [4\text{-}4]$$

where $R_1 = R_2 = R_3 = R$ and $C_1 = C_2 = C_3 = C$.

Exercise 4-2:

(a) Determine the value of R_f necessary for the circuit in Fig. 4-10 to operate as an oscillator. Use $R_1 = R_2 = R_3 = R = 10$ kΩ and $C_1 = C_2 = C_3 = C = 0.001$ μF.

(b) Calculate the frequency of oscillation.

[Answers: (a) 290 kΩ, (b) 5.6 kHz]

Derivations of Selected Equations:

Equations 4-1 and 4-2:

$$\frac{V_{out}}{V_{in}} = \frac{R(-jX)/(R - jX)}{(R - jX) + R(-jX)/(R - jX)} = \frac{R(-jX)}{(R - jX)^2 - jRX}$$

Multiplying the numerator and denominator by j,

$$\frac{V_{out}}{V_{in}} = \frac{RX}{j(R - jX)^2 + RX} = \frac{RX}{RX + j(R^2 - j2RX - X^2)}$$

$$= \frac{RX}{RX + jR^2 + 2RX - jX^2} = \frac{RX}{3RX + j(R^2 - X^2)}$$

For a 0° phase angle there can be no j term. Recall from complex numbers in ac theory that a *nonzero* angle is associated with a complex number having a j term. Therefore, at f_r the j term is 0.

$$R^2 - X^2 = 0$$

Thus,

$$\frac{V_{out}}{V_{in}} = \frac{RX}{3RX}$$

Cancelling yields

$$\frac{V_{out}}{V_{in}} = \frac{1}{3}$$

$$R^2 - X^2 = 0$$
$$R^2 = X^2$$
$$R = X$$

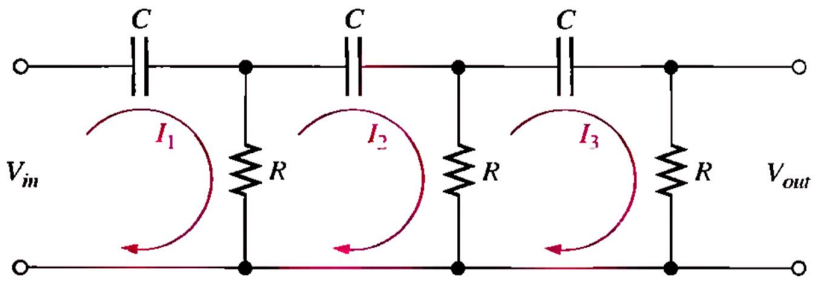
Since $X = \dfrac{1}{2\pi f_r C}$,

$$R = \frac{1}{2\pi f_r C}$$

$$f_r = \frac{1}{2\pi RC}$$

Equations 4-3 and 4-4:

The feedback circuit in the phase-shift oscillator consists of three *RC* stages, An expression for the attenuation is derived using the mesh analysis method for the loop assignment shown. All *R*s are equal in value, and all *C*s are equal in value.



$$
\begin{aligned}
(R - j1/2\pi fC)I_1 - RI_2 + 0I_3 &= V_{in} \\
-RI_1 + (2R - j1/2\pi fC)I_2 - RI_3 &= 0 \\
0I_1 - RI_2 + (2R - j1/2\pi fC)I_3 &= 0
\end{aligned}
$$

In order to get V_{out}, we must solve for I_3 using determinants:

$$
I_3 = \frac{\begin{vmatrix} (R - j1/2\pi fC) & -R & V_{in} \\ -R & (2R - j1/2\pi fC) & 0 \\ 0 & -R & 0 \end{vmatrix}}{\begin{vmatrix} (R - j1/2\pi fC) & -R & 0 \\ -R & (2R - j1/2\pi fC) & -R \\ 0 & -R & (2R - j1/2\pi fC) \end{vmatrix}}
$$

$$
I_3 = \frac{R^2 V_{in}}{(R - j1/2\pi fC)(2R - j1/2\pi fC)^2 - R^2(2R - j1/2\pi fC) - R^2(R - 1/2\pi fC)}
$$

$$
\frac{V_{out}}{V_{in}} = \frac{RI_3}{V_{in}}
$$

$$
= \frac{R^3}{(R - j1/2\pi fC)(2R - j1/2\pi fC)^2 - R^3(2 - j1/2\pi fRC) - R^3(1 - 1/2\pi fRC)}
$$

$$
= \frac{R^3}{R^3(1 - j1/2\pi fRC)(2 - j1/2\pi fRC)^2 - R^3[(2 - j1/2\pi fRC) - (1 - j1/2\pi fRC)]}
$$

$$
= \frac{R^3}{R^3(1 - j1/2\pi fRC)(2 - j1/2\pi fRC)^2 - R^3(3 - j1/2\pi fRC)}
$$

$$
\frac{V_{out}}{V_{in}} = \frac{1}{(1 - j1/2\pi fRC)(2 - j1/2\pi fRC)^2 - (3 - j1/2\pi fRC)}
$$

Expanding and combining the real terms and the j terms separately.

$$
\frac{V_{out}}{V_{in}} = \frac{1}{\left(1 - \frac{5}{4\pi^2 f^2 R^2 C^2}\right) - j\left(\frac{6}{2\pi fRC} - \frac{1}{(2\pi f)^3 R^3 C^3}\right)}
$$

For oscillation in the phase-shift amplifier, the phase shift through the *RC* circuit must equal 180°. For this condition to exist, the *j* term must be 0 at the frequency of oscillation f_r.

$$\frac{6}{2\pi f_r RC} - \frac{1}{(2\pi f_r)^3 R^3 C^3} = 0$$

$$\frac{6(2\pi)^2 f_r^2 R^2 C^2 - 1}{(2\pi)^3 f_r^3 R^3 C^3} = 0$$

$$6(2\pi)^2 f_r^2 R^2 C^2 - 1 = 0$$

$$f_r^2 = \frac{1}{6(2\pi)^2 R^2 C^2}$$

$$f_r = \frac{1}{2\pi\sqrt{6}RC}$$

Since the *j* term is 0,

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 - \dfrac{5}{4\pi^2 f_r^2 R^2 C^2}} = \frac{1}{1 - \dfrac{5}{\left(\dfrac{1}{\sqrt{6}RC}\right)^2 R^2 C^2}} = \frac{1}{1 - 30} = -\frac{1}{29}$$

The negative sign results from the 180° inversion. Thus, the value of attenuation for the feedback circuit is

$$B = \frac{1}{29}$$

4.4 Oscillators with LC Feedback Circuits:

Although the RC feedback oscillators, particularly the Wien bridge, are generally suitable for frequencies up to about 1 MHz, LC feedback elements are normally used in oscillators that require higher frequencies of oscillation. Also, because of the frequency limitation (lower unity-gain frequency) of most op-amps, discrete transistors (BJT or FET) are often used as the gain element in LC oscillators. This section introduces several types of resonant LC feedback oscillators: the Colpitts, Clapp, Hartley, Armstrong, and crystal-controlled oscillators.

4.4.1 Colpitts Oscillators:

One basic type of resonant circuit feedback oscillator is the ***Colpitts***, named after its inventor-as are most of the others we cover here. As shown in Fig. 4-11, this type of oscillator uses an LC circuit in the feedback loop to provide the necessary phase shift and to act as a resonant filter that passes only the desired frequency of oscillation.

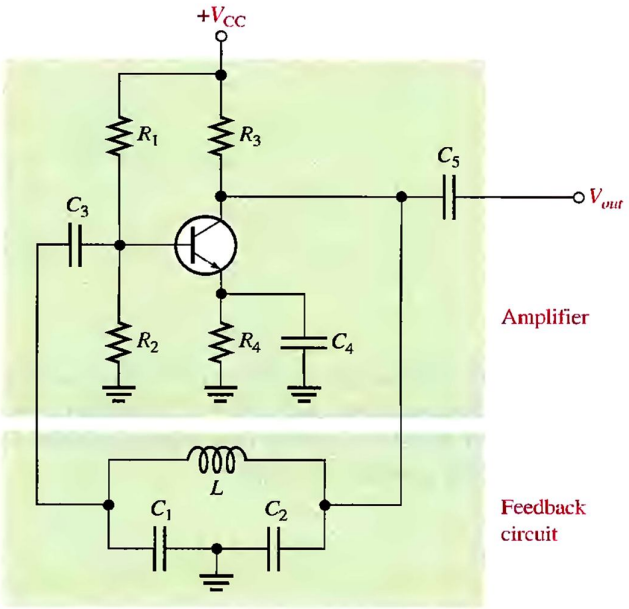


Fig. 4-11

The approximate frequency of oscillation is the resonant frequency of the LC circuit and is established by the values of C_1, C_2, and L according to this familiar formula:

$$f_r \cong \frac{1}{2\pi\sqrt{LC_T}} \qquad [4\text{-}5]$$

where C_T is the total capacitance. Because the capacitors effectively appear in series around the tank circuit, the total capacitance (C_T) is

$$C_T = \frac{C_1 C_2}{C_1 + C_2}$$

The attenuation, B, of the resonant feedback circuit in the Colpitts oscillator is basically determined by the values of C_1 and C_2. Fig. 4-12 shows that the circulating tank current is through both C_1, and C_2 (they are effectively in series). The voltage developed across C_2 is the oscillator's output voltage (V_{out}) and the voltage developed across C_1 is the feedback voltage (V_f), as indicated. The expression for the attenuation (B) is

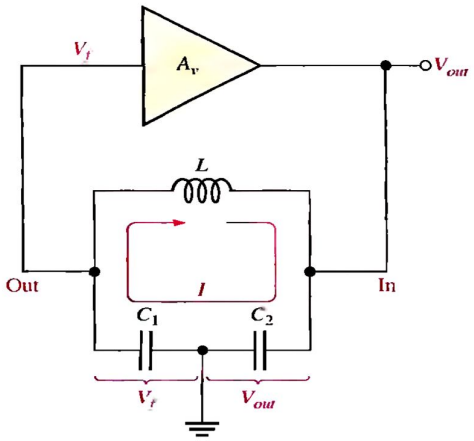


Fig. 4-12

$$B = \frac{V_f}{V_{out}} \cong \frac{IX_{C1}}{IX_{C2}} = \frac{X_{C1}}{X_{C2}} = \frac{1/(2\pi f_r C_1)}{1/(2\pi f_r C_2)}$$

Cancelling the $2\pi f_r$ terms gives

$$B = \frac{C_2}{C_1}$$

As we know, a condition for oscillation is $A_vB = 1$,

$$A_v = \frac{C_1}{C_2} \qquad [4\text{-}6]$$

where A_v, is the voltage gain of the amplifier, which is represented by the triangle in Fig. 4-12. With this condition met, $A_vB = (C_1/C_2)(C_2/C_1) = 1$. Actually, for the oscillator to be self-starting, A_vB must be greater than 1 (that is, $A_vB > 1$). Therefore, the voltage gain must be made slightly greater than C_1/C_2,

$$A_v > \frac{C_1}{C_2}$$

As indicated in Fig. 4-13, the input impedance of the amplifier acts as a load on the resonant feedback circuit and reduces the Q of the circuit. Recall from our study of resonance that the resonant frequency of a parallel resonant circuit depends on the Q, according to the following formula:

$$f_r = \frac{1}{2\pi\sqrt{LC_T}}\sqrt{\frac{Q^2}{Q^2+1}} \qquad [4\text{-}7]$$

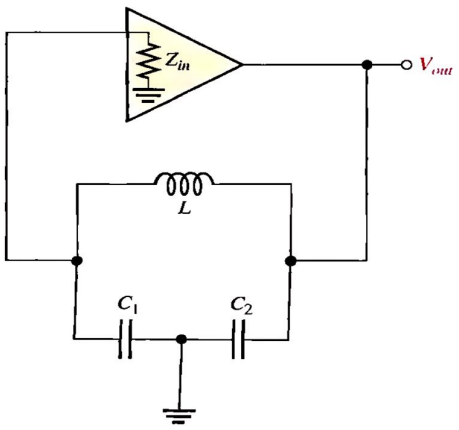


Fig. 4-13

A FET can be used in place of a BJT, as shown in Fig. 4-14, to minimize the loading effect of the transistor's input impedance. Recall that FETs have much higher input impedances than do bipolar junction transistors. Also, when an external load is connected to the oscillator output, as shown in Fig. 4-15(a), f_r, may decrease, again because of a reduction in Q. This happens if the load resistance is too small. In some cases, one way to eliminate the effects of a load resistance is by transformer coupling, as indicated in Fig. 4-15(b).

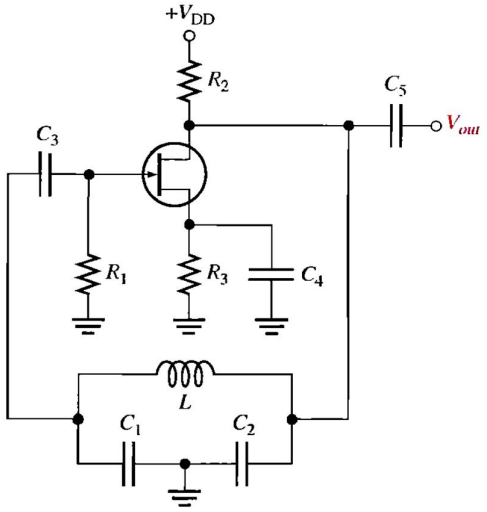
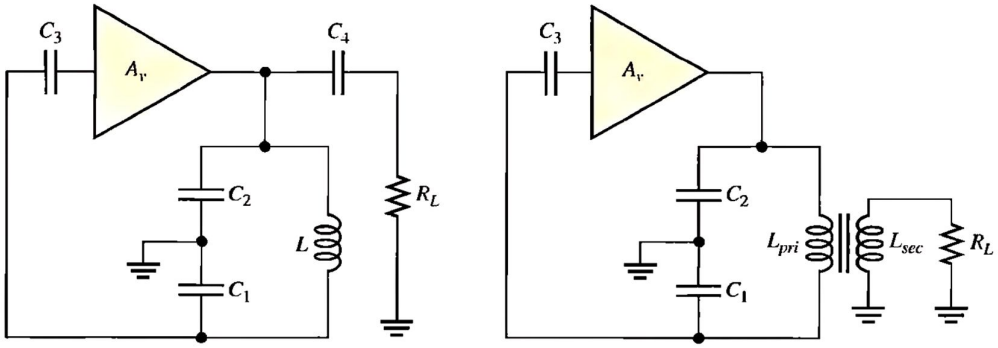


Fig. 4-14



(a) (b)

Fig. 4-15

Exercise 4-3:

(a) Determine the frequency for the oscillator in Fig. 4-11. Assume there is negligible loading on the feedback circuit and that its Q is greater than 10. Use L = 50 mH, C_1 = 0.1 µF, and C_2 = 0.01 µF.

(b) Find the frequency if the oscillator is loaded to a point where the Q drops to 8.

[Answers: (a) 7.46 kHz, (b) 7.40 kHz]

4.4.2 Clapp Oscillators:

The ***Clapp*** oscillator is a variation of the Colpitts. The basic difference is an additional capacitor, C_3, in series with the inductor in the resonant feedback circuit, as shown in Fig. 4-16. Since C_3 is in series with C_1 and C_2 around the tank circuit, the total capacitance is

$$C_T = \frac{1}{\frac{1}{C_1}+\frac{1}{C_2}+\frac{1}{C_3}}$$

and the approximate frequency of oscillation ($Q > 10$) is

$$f_r = \frac{1}{2\pi\sqrt{LC_T}} \qquad [4\text{-}8]$$

If C_3 is much smaller than C_1 and C_2, then C_3 almost entirely controls the resonant frequency ($f_r = 1/(2\pi\sqrt{LC_3})$). Since C_1 and C_2 are both connected to ground at one end, the junction capacitance of the transistor and other stray capacitances appear in parallel with C_1 and C_2 to ground, altering their effective values. C_3 is not affected, however, and thus provides a more accurate and stable frequency of oscillation.

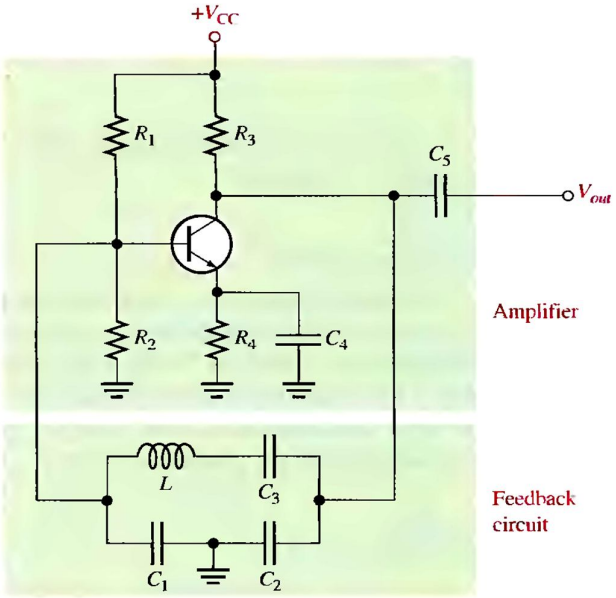


Fig. 4-16

4.4.3 Hartley Oscillators:

The ***Hartley*** oscillator is similar to the Colpitts except that the feedback circuit consists of two series inductors and a parallel capacitor as shown in Fig. 4-17.

In this circuit, the frequency of oscillation for $Q > 10$ is

$$f_r \cong \frac{1}{2\pi\sqrt{L_T C}} \qquad [4\text{-}9]$$

where $L_T = L_1 + L_2$. The inductors act in a role similar to C_1 and C_2 in the Colpitts to determine the attenuation, B, of the feedback circuit.

$$B = \frac{L_1}{L_2}$$

To assure start-up of oscillation, A_v, must be greater than $1/B$.

$$A_v > \frac{L_2}{L_1} \qquad [4\text{-}10]$$

Loading of the tank circuit has the same effect in the Hartley as in the Colpitts; that is, the Q is decreased and thus f_r decreases.

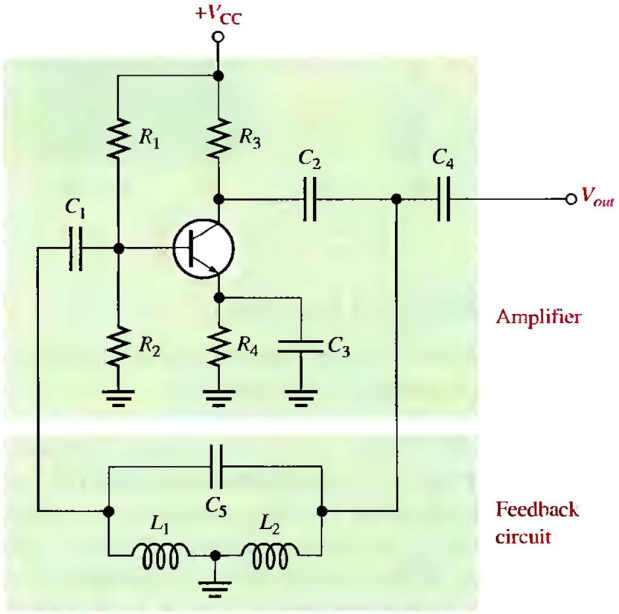


Fig. 4-17

4.4.4 Armstrong Oscillators:

This type of LC feedback oscillator uses transformer coupling to feed back a portion of the signal voltage, as shown in Fig. 4-18. It is sometimes called a "***tickler***" oscillator in reference to the transformer secondary or "tickler coil" that provides the feedback to keep the oscillation going. The ***Armstrong*** is less common than the Colpitts, Clapp, and Hartley, mainly because of the disadvantage of transformer size and cost. The frequency of oscillation is set by the inductance of the primary winding (L_{pri}) in parallel with C_1.

$$f_r = \frac{1}{2\pi\sqrt{L_{pri}C_1}} \qquad [4\text{-}11]$$

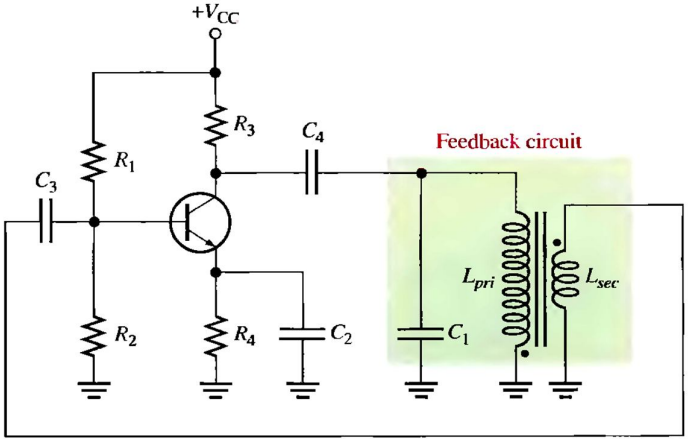
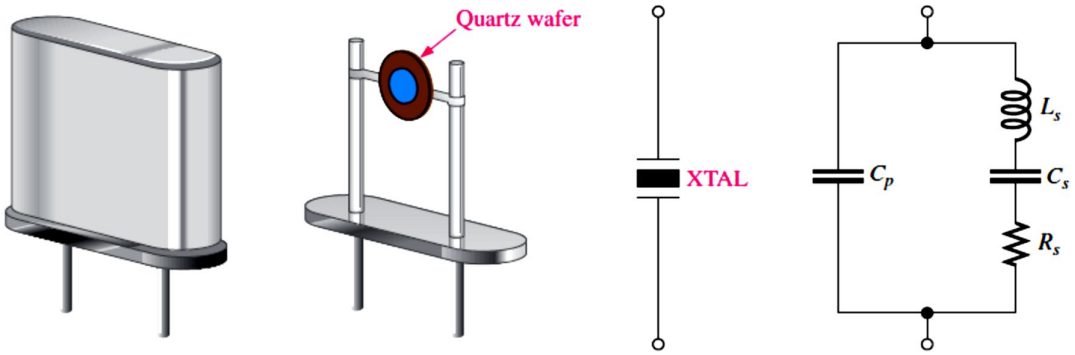


Fig. 4-18

4.4.5 Crystal-Controlled Oscillators:

The most stable and accurate type of feedback oscillator uses a ***piezoelectric crystal*** in the feedback loop to control the frequency. ***Quartz*** is one type of crystalline substance found in nature that exhibits a property called the ***piezoelectric effect***. When a changing mechanical stress is applied across the crystal to cause it to vibrate, a voltage develops at the frequency of mechanical vibration. Conversely, when an ac voltage is applied across the crystal, it vibrates at the frequency of the applied voltage. The greatest vibration occurs at the crystal's natural resonant frequency, which is determined by the physical dimensions and by the way the crystal is cut.

Crystals used in electronic applications typically consist of a quartz wafer mounted between two electrodes and enclosed in a protective "can" as shown in Fig. 4-19(a) and (b). A schematic symbol for a crystal is shown in Fig. 4-19(c), and an equivalent RLC circuit for the crystal appears in Fig. 4-19(d). The crystal's equivalent circuit is a series-parallel RLC circuit and can operate in either series resonance or parallel resonance. The impedance versus frequency of the crystal is shown in Fig. 4-20. At the series resonant frequency, f_1, the inductive reactance is cancelled by the reactance of C_s. The remaining series resistor, R_s, determines the impedance of the crystal. Parallel resonance occurs when the inductive reactance and the reactance of the parallel capacitance, C_p, are equal. The parallel resonant frequency, f_2, is usually at least 1 kHz higher than the series resonant frequency. A great advantage of the crystal is that it exhibits a very high Q (Qs with values of several thousand are typical).



(a) (b) (c) (d)

Fig. 4-19

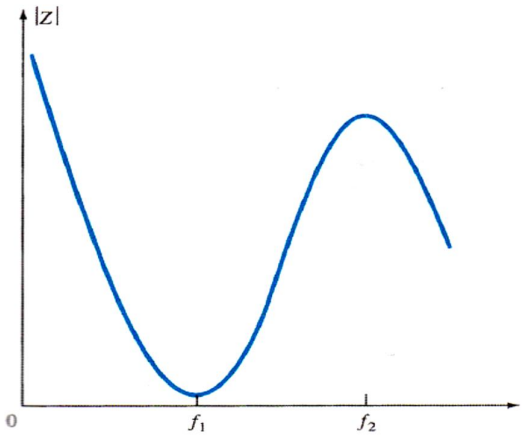


Fig. 4-20

As mentioned above, the series resonance occurs, in crystal, when $X_{Cs} = X_{Ls}$. The formula for this series resonant frequency is

$$f_1 = f_s = \frac{1}{2\pi\sqrt{LC_s}} \quad [4\text{-}12]$$

Also, the parallel resonance occurs, at higher frequency, when $X_{Cp} = X_{Ls}$. The formula for this parallel resonant frequency is

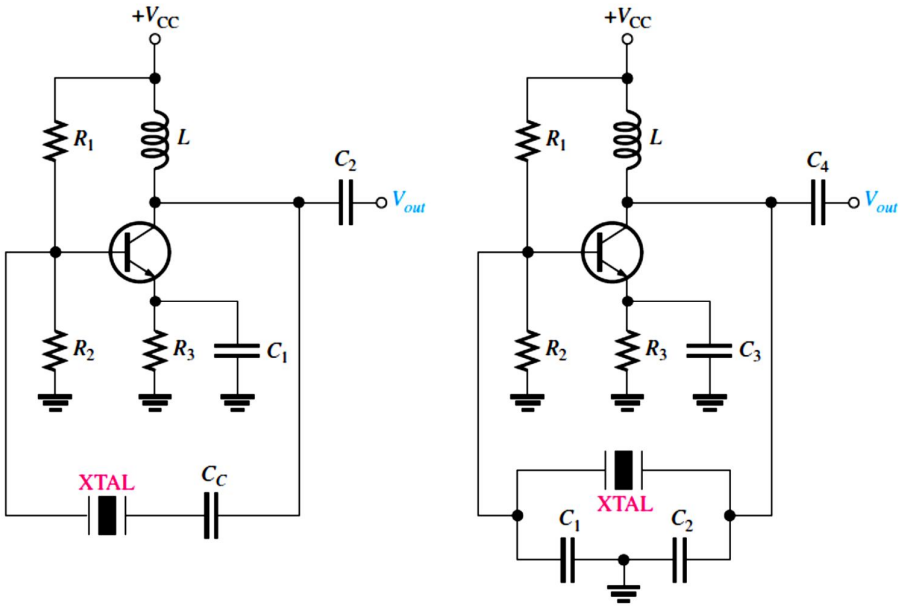
$$f_2 = f_p = \frac{1}{2\pi\sqrt{LC_T}} \quad [4\text{-}13]$$

where C_T is the series combinations of C_s and C_p, the equivalent C_T is

$$C_T = \frac{C_s C_p}{C_s + C_p}$$

An oscillator that uses a crystal as a series resonant tank circuit is shown in Fig. 4-21(a). The impedance of the crystal is minimum at the series resonant frequency, thus providing maximum feedback. The crystal tuning capacitor, C_C, is used to "fine tune" the oscillator frequency by "pulling" the resonant frequency of the crystal slightly up or down.

A modified Colpitts configuration is shown in Fig. 4-21(b) with a crystal acting as a parallel resonant tank circuit. The impedance of the crystal is maximum at parallel resonance, thus developing the maximum voltage across the capacitors. The voltage across is fed back to the input.



(a) (b)

Fig. 4-21

Piezoelectric crystals can oscillate in either of two modes-fundamental or overtone. The fundamental frequency of a crystal is the lowest frequency at which it is naturally resonant. The fundamental frequency depends on the crystal's mechanical dimensions, type of cut, and other factors, and is inversely proportional to the thickness of the crystal slab. Because a slab of crystal cannot be cut too thin without fracturing, there is an upper limit on the fundamental frequency. For most crystals, this upper limit is less than

20 MHz. For higher frequencies, the crystal must be operated in the overtone mode. Overtones are approximate integer multiples of the fundamental frequency. The overtone frequencies are usually, but not always, odd multiples (3, 5, 7, …) of the fundamental. Many crystal oscillators are available in integrated circuit packages.

Exercise 4-4:

A crystal has these values: L_s = 3 H, C_s = 0.05 pF, R_s = 2 kΩ, and C_p = 10 pF. Calculate the f_s and f_p of the crystal to three significant digits.

[Answers: 411 kHz, 412 kHz]

4.5 Relaxation (Nonsinusoidal) Oscillators:

The second major category of oscillators is the relaxation oscillator. Relaxation oscillators use an RC timing circuit and a device that changes states to generate a periodic waveform. In this section, we will learn about several circuits that are used to produce a waveform that is generally a square wave or other nonsinusoidal (triangular) waveform. Typically, a relaxation oscillator uses a Schmitt trigger or other device that changes states to alternately charge and discharge a capacitor through a resistor.

4.5.1 Hysteresis and Schmitt Trigger Oscillators:

Hysteresis is a property that means a device behaves differently when its input is increasing from the way it behaves when its input is decreasing. In the context of a voltage comparator, hysteresis means that the output will switch when the input increases to one level but will not switch back until the input falls below a different level. In some applications, hysteresis is a desirable characteristic because it prevents the comparator from switching back and forth in response to random noise fluctuations in the input.

Fig. 4-22(a) shows how hysteresis can be introduced into comparator operation. In this case, the input is connected to the inverting terminal and a voltage divider is connected across the noninverting terminal between v_o and a fixed reference voltage V_{REF} (which may be 0). Fig 4-22(b) shows the resulting ***transfer characteristic*** (called a ***hysteresis loop***). This characteristic shows that the output switches to $+V_{max}$ when v_{in} falls below a lower rigger level (LTL), but will not switch to $-V_{max}$ unless v_{in}, rises past an upper trigger level (UTL). The arrows indicate the portions of the characteristic followed when the input is increasing (upper line) and when it is decreasing (lower line). A comparator having this characteristic is called a ***Schmitt trigger***.

We can derive expressions for UTL and LTL using the superposition principle. Suppose first that the comparator output is shorted to ground. Then

$$v^+ = \frac{R_2}{R_1+R_2}V_{REF} \quad (v_o = 0)$$

When V_{REF} is 0, we find

$$v^+ = \frac{R_1}{R_1+R_2}v_o \quad (V_{REF} = 0)$$

Therefore, when the output is at its negative limit ($v_o = -V_{max}$),

$$v^+ = \frac{R_2}{R_1+R_2}V_{REF} + \frac{R_1}{R_1+R_2}(-V_{max})$$

MODULE 5

CS 205

Power Amplifiers

3.1 General Concepts:

A ***power amplifier*** is one that is designed to deliver a large amount of power to a load. To perform this function, a power amplifier must itself be capable dissipating large amounts of power; so that the heat generated when it is operated at high current and voltage levels is released into the surroundings at a rate fast enough to prevent destructive temperature buildup. Power amplifiers typically contain bulky components having large surface areas to enhance heat transfer to the environment. A power transistor is a discrete device with a large surface area and a metal case.

A power amplifier is often the last stage of an amplifier system designed to modify signal characteristics referred to as signal conditioning. It is designed at least one of its semiconductor components, typically a power transistor, can be operated over substantially the entire range of its output characteristics, from saturation to cutoff. This mode of operation is called ***large-signal operation***. The term "large-signal operation" is also applied to devices used in digital switching circuits. In these applications, the output level switches between "high" and "low" (cutoff and saturation), but remains in those states most of the time. Power dissipation is therefore not a problem. On the other hand, the variations in the output level of a power amplifier occur in the active region, between the two extremes of saturation and cutoff, so a substantial amount of power is dissipated.

3.2 Transistor Power Dissipation:

A power is the rate at which energy is consumed or dissipated (1 watt = 1 joule/second). If the rate at which heat energy is dissipated in a device is less than the rate at which it is generated, the temperature of the device must rise. In electronic devices, electrical energy is converted to heat energy at a rate given by $P = VI$ watts, and temperature rises when this heat energy is not removed at a comparable rate. Since semiconductor material is irreversibly damaged when subjected to temperatures beyond a certain limit, temperature is the parameter that ultimately limits the amount of power a semiconductor device can handle.

Transistor manufacturers specify the maximum permissible junction temperature and the maximum permissible power dissipation that a transistor can withstand. In normal transistor operation, the collector-base junction is reverse biased and has, on average, a large voltage across it, while the base-emitter junction has a small forward-biasing voltage. Consequently, most of the heat generated in a transistor is produced at the collector-base junction. The total power dissipated at the junctions is

$$P_d = v_{cb}i_c + v_{be}i_e \approx (v_{cb} + v_{be})i_c \approx v_{ce}i_c.$$

Fig. 3-1 shows a simple common-emitter amplifier and its dc load line plotted on I_C–V_{CE} axes. As the amplifier output changes in response to an input signal, the collector current and voltage undergo variations along the load line and intersect different hyperbolas of power dissipation. It is clear that the power dissipation changes as the amplifier output changes. For safe operation, the load line must lie below and to the left of the hyperbola corresponding to the maximum permissible power dissipation.

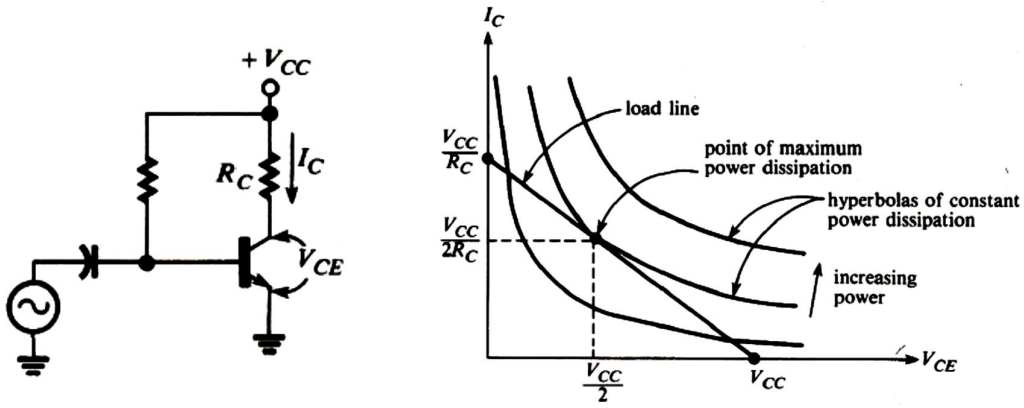


Fig. 3-1

It can be shown that the point of maximum power dissipation occurs at the center of the load line, where $V_{CE} = V_{CC}/2$ and $I_C = V_{CC}/2R_C$ (see Fig. 3-1). Therefore, the maximum power dissipation is

$$P_d(\text{max}) = \left(\frac{V_{CC}}{2}\right)\left(\frac{V_{CC}}{2R_C}\right) = \frac{V_{CC}^2}{4R_C} \qquad [3\text{-}1]$$

To ensure that the load line lies below the hyperbola of maximum dissipation, we therefore require that

$$\frac{V_{CC}^2}{4R_C} < P_d(\text{max}) \quad \Rightarrow$$

$$R_C > \frac{V_{CC}^2}{4P_d(\text{max})} \qquad [3\text{-}2]$$

where P_d(max) is the manufacturer's specified maximum dissipation at a specified ambient temperature.

Exercise 3-1:

The amplifier in Fig. 3-1 is to be operated with $V_{CC} = 20$V and $R_C = 1$ kΩ.

(a) What maximum power dissipation rating should the transistor have?

(b) If an increase in ambient temperature reduces the maximum rating found in (a) by a factor of 2, what new value of R_C should be used to ensure safe operation?

[Answers: (a) 0.1 W, (b) 2 kΩ]

3.3 Class-A Power Amplifiers:

All the small-signal amplifiers have been designed so that output voltage can vary in response to both positive and negative inputs; that is, the amplifiers are biased so that under normal operation the output never saturates or cuts off. An amplifier that has that property is called a ***class-A*** amplifier. More precisely, an amplifier is class A if its output remains in the active region during a complete cycle (one full period) of a sine-wave input signal.

Fig. 3-2 shows a typical class-A amplifier and its input and output waveforms. In this case, the transistor is biased at $V_{CE} = V_{CC}/2$, which is midway between saturation and cutoff, and which permits maximum output voltage swing. The output can vary through (approximately) a full V_{CC} volts, peak-to-peak. The output is in the transistor's active region during a full cycle (360°) of the input sine wave.

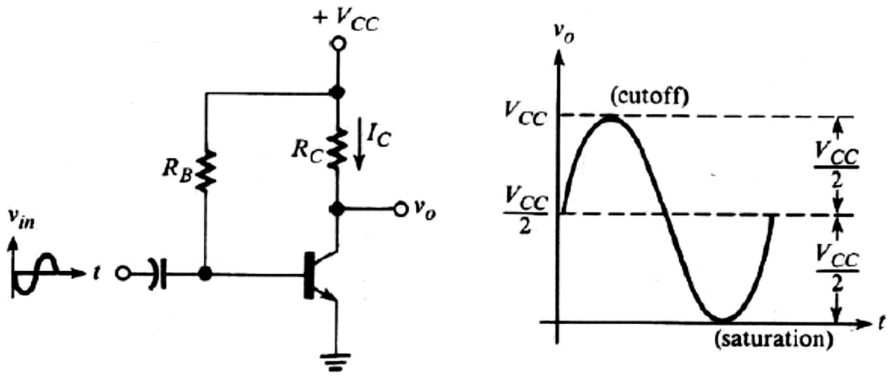


Fig. 3-2

The ***efficiency*** of a power amplifier is defined to be

$$\eta = \frac{\text{average signal power delivered to load}}{\text{average power drawn from dc source}} \qquad [3\text{-}3]$$

The numerator of Eqn. [3-3] is average signal power, that is, average ac power, excluding any dc or bias components in the load. Recall that when voltages and currents are sinusoidal, average ac power can be calculated using any of the following relations:

$$P = V_{rms}I_{rms} = V_P I_P/2 = V_{PP}I_{PP}/8$$
$$P = I_{rms}^2 R = I_P^2 R/2 = I_{PP}^2 R/8 \qquad [3\text{-}4]$$
$$P = V_{rms}^2/R = V_P^2/2R = V_{PP}^2/8R$$

The efficiency of a class-A amplifier is 0 when no signal is present. The amplifier is said to be in standby when no signal is applied to its input. We will now derive a general expression for the efficiency of the class-A amplifier shown in Fig. 3-2. In doing so, we will not consider the small power consumed in the base-biasing circuit, i.e., the power at the input side: $I_B^2 R_B + v_{be} i_b$.

3.3.1 Series-Fed Class-A Power Amplifiers:

Fig. 3-3 shows the voltages and currents used in our analysis. Notice that resistance R is considered to be the load. We will refer to this configuration as a ***series-fed*** class-A amplifier, and we will consider ***capacitor-*** and ***transformer-coupled*** loads in a later discussion.

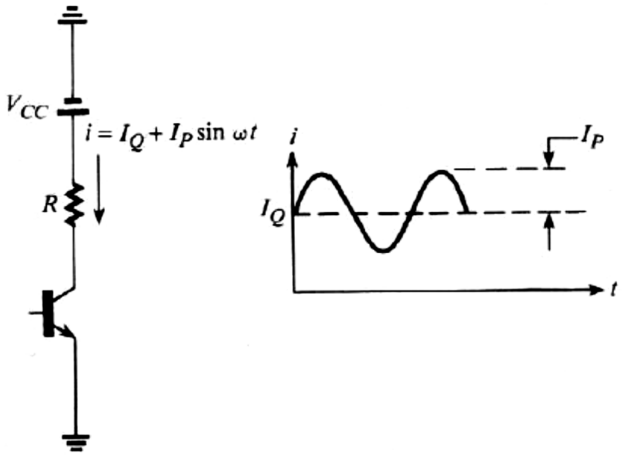


Fig. 3-3

The instantaneous power from the dc supply is

$$P_S(t) = V_{CC}i = V_{CC}(I_Q + I_P \sin \omega t) = V_{CC}I_Q + V_{CC}I_P \sin \omega t.$$

Since the average value of the sine term is 0, the average power from the dc supply is

$$P_S = V_{CC}I_Q.$$

The average signal power in load resistor R is, from Eqn. [3-4],

$$P_R = I_P^2 R/2 .$$

Therefore, by Eqn. [3-3],

$$\eta = \frac{P_R}{P_S} = \frac{I_P^2 R}{2V_{CC}I_Q} \qquad [3\text{-}5]$$

We see again that the efficiency is 0 under no-signal conditions ($I_P = 0$) and that efficiency rises as the peak signal level I_P increases. The maximum possible efficiency occurs when I_P has its maximum possible value without distortion. When the bias point is at the center of the load line, as shown in Fig. 3-1, the quiescent current is one-half the saturation current, and the output current can swing through the full range from 0 to V_{CC}/R amps without distorting (clipping). Thus, the maximum undistorted peak current is also one-half the saturation current:

$$I_Q = I_P = V_{CC}/2R.$$

Substituting this equation into Eqn. [3-5], we find the maximum possible efficiency of the series-fed, class-A amplifier:

$$\eta(\text{max}) = \frac{(V_{CC}/2R)^2 R}{2V_{CC}(V_{CC}/2R)} = 0.25$$

This result shows that the best possible efficiency of a series-fed, class-A amplifier is undesirably small: only 1/4 of the total power consumed by the circuit is delivered to the load, under optimum conditions. For that reason, this type of amplifier is not widely used in heavy power applications. The principal advantage of the class-A amplifier is that it generally produces less signal distortion than some of the other, more efficient classes that we will consider later.

Another type of efficiency used to characterize power amplifiers relates signal power to total power dissipated at the collector. Called ***collector efficiency***, its practical significance stems from the fact that a major part of the cost and bulk of a power amplifier is invested in the output device itself and the means used to cool it. Therefore, it is desirable to maximize, the ratio of signal power in the load to power consumed by the device. Collector efficiency η_c is defined by

$$\eta_c = \frac{\text{average signal power delivered to load}}{\text{average power dissipated at collector}} \qquad [3\text{-}6]$$

The average power P_C dissipated at the collector of the class-A amplifier in Fig. 3-3 is the product of the dc (quiescent) voltage and current:

$$P_C = V_Q I_Q = (V_{CC} - I_Q R)I_Q.$$

Therefore,

$$\eta_c = \frac{I_P^2 R/2}{(V_{CC} - I_Q R)I_Q} \qquad [3\text{-}7]$$

The maximum value of η_c occurs when I_P is maximum, $I_P = I_Q = V_{CC}/2R$, as previously discussed. Substituting these values into Eqn. [3-7] gives

$$\eta_c(\text{max}) = \frac{(V_{CC}/2R)^2 R/2}{(V_{CC} - V_{CC}/2)V_{CC}/2R} = 0.5$$

3.3.2 Capacitor-Coupled Class-A Power Amplifiers:

Fig. 3-4 shows the output side of a class-A amplifier with capacitor-coupled load R_L. Also shown are the dc and ac load lines that result. In this case, the average power delivered to the load is

$$P_L = I_{PL}^2 R_L/2,$$

where I_{PL} is the peak ac load current. The average power from the dc source is computed in the same way as for the series-fed amplifier: $P_S = V_{CC}I_Q$, so the efficiency is

$$\eta = \frac{I_{PL}^2 R_L}{2V_{CC}I_Q} \qquad [3\text{-}8]$$

As in the case of the series-fed amplifier, the efficiency is 0 under no-signal (standby) conditions and increases with load current I_{PL}.

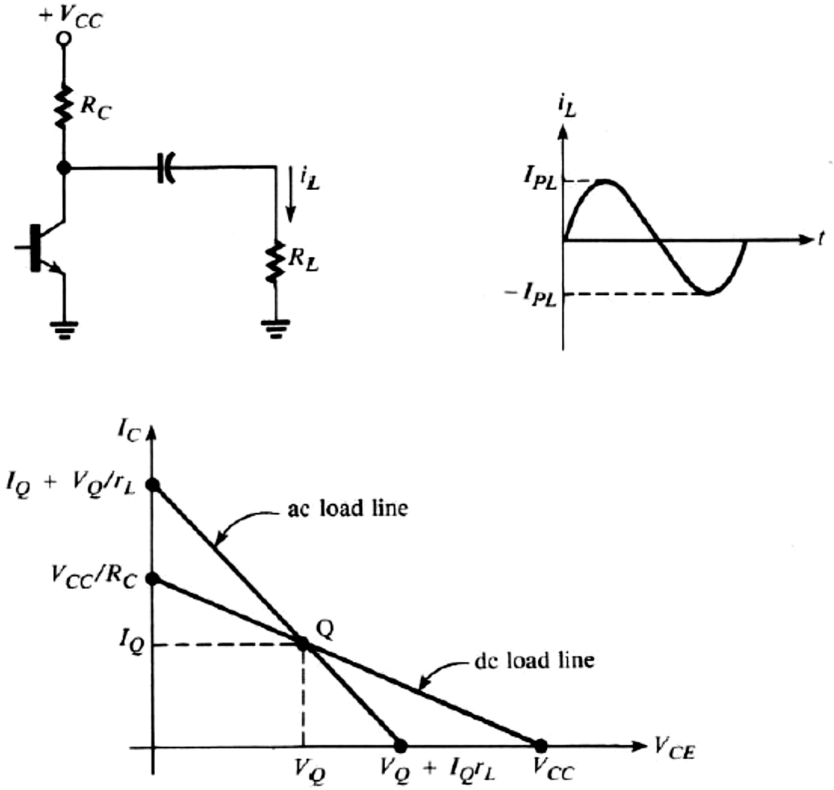


Fig. 3-4

Recall that maximum output swing can be achieved by setting the Q-point in the center of the ac load line, at

$$I_Q = \frac{V_{CC}}{R_C + r_L}.$$

The peak collector current under those circumstances is $V_{CC}/(R_C + r_L)$. Neglecting the transistor output resistance, the portion of the collector current that flows in R_L is, by the current-divider rule,

$$I_{PL} = \left(\frac{V_{CC}}{R_C + r_L}\right)\left(\frac{R_C}{R_C + R_L}\right).$$

The average ac power in the load resistance R_L is then

$$P_L = \frac{I_{PL}^2 R_L}{2} = \left[\left(\frac{V_{CC}}{R_C + r_L}\right)\left(\frac{R_C}{R_C + R_L}\right)\right]^2 (R_L/2).$$

The average power supplied from the dc source is

$$P_S = V_{CC} I_Q = \frac{V_{CC}^2}{R_C + r_L}.$$

Therefore, the efficiency under the conditions of maximum possible undistorted output is

$$\eta = \frac{P_L}{P_S} = \frac{\left[\left(\frac{V_{CC}}{R_C + r_L}\right)\left(\frac{R_C}{R_C + R_L}\right)\right]^2 (R_L/2)}{\frac{V_{CC}^2}{R_C + r_L}} \Rightarrow$$

$$\eta = \frac{R_C R_L}{2(R_C + 2R_L)(R_C + R_L)} = \frac{r_L}{2(R_C + 2R_L)} \qquad [3\text{-}9]$$

Eqn. [3-9] shows that the efficiency depends on both R_C and R_L. In practice, R_L is a fixed and known value of load resistance, will the value of R_C is selected by the designer. Using calculus (differentiating Eqn. [3-9] with respect to R_C), it can be shown that η is maximized by setting $R_C = \sqrt{2} R_L$. With this value of R_C, the maximum efficiency is

$$\eta(\text{max}) = 0.0858$$

Another criterion for choosing R_C is to select its value so that maximum power is transferred to the load. Since the transistor output resistance has been neglected, maximum power transfer occurs when $R_C = R_L = R$. Under that circumstance, $r_L = R/2$, and, by substituting into Eqn. [3-9], we find the maximum possible efficiency with maximum power transfer to be

$$\eta(\text{max}) = 0.0833 \quad \text{(max power transfer)}.$$

It is interesting to note that the efficiency under maximum power transfer (0.0833) is somewhat less than that which can be achieved (0.0858) without regard to power transfer. In either case, the maximum efficiency is substantially less than that attainable in the series-fed class-A amplifier.

Exercise 3-2:

The class-A amplifier shown in Fig. 3-5 is biased at V_{CE} = 12 V. The output voltage is the maximum possible without distortion. Find

(a) the average power from the dc supply,
(b) the average power delivered to the load,
(c) the efficiency, and
(d) the collector efficiency.

[Answers: (a) 5.76 W, (b) 0.36 W, (c) 0.0625, (d) 0.125]

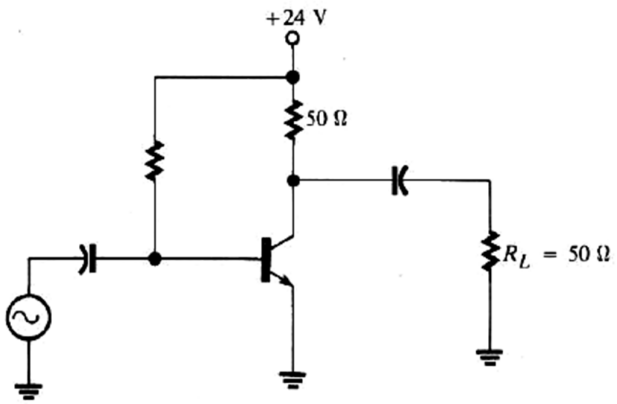


Fig. 3-5

3.3.3 Transformer-Coupled Class-A Power Amplifiers:

Output transformers are used to couple power amplifiers to their loads. As in other coupling applications, the advantages of a transformer are that it provides an opportunity to achieve impedance matching for maximum power transfer and that it blocks the flow of dc current in a load.

Fig. 3-6 shows a transformer used to couple the output of a transistor to load R_L. Also shown are the dc and ac load lines for the amplifier. Here we assume that the dc resistance of the primary winding is negligibly small, so the dc load line is vertical (slope = $-1/R_{dc} = -\infty$). Recall that the ac resistance r_L reflected to the primary side is

$$r_L = (N_p/N_s)^2 R_L \qquad [3\text{-}10]$$

where N_p and N_s, are the numbers of turns on the primary and secondary windings, respectively. As shown in the figure, the slope of the ac load line is $-1/r_L$.

Since we are assuming that there is negligible resistance in the primary winding, there is no dc voltage drop across the winding, and the quiescent collector voltage is therefore V_{CC} volts, as shown in Fig. 3-6. Conventional base-bias circuitry (not shown in the figure) is used to set the quiescent collector current I_Q. The Q-point is the point on the dc load line at which the collector current equals I_Q.

Since V_{CE} cannot be negative, the maximum permissible decrease in V_{CE} below its quiescent value is $V_Q = V_{CC}$ volts. Thus, the maximum possible peak value of V_{CE} is V_{CC} volts. To achieve maximum peak-to-peak output variation, the intercept of the ac load line on the V_{CE}-axis should therefore be $2V_{CC}$ volts, as shown in Fig. 3-6. The quiescent current I_Q is selected so that the ac load line, a line having slope $-1/r_L$, intersects the V_{CE}-axis at $2V_{CC}$ volts.

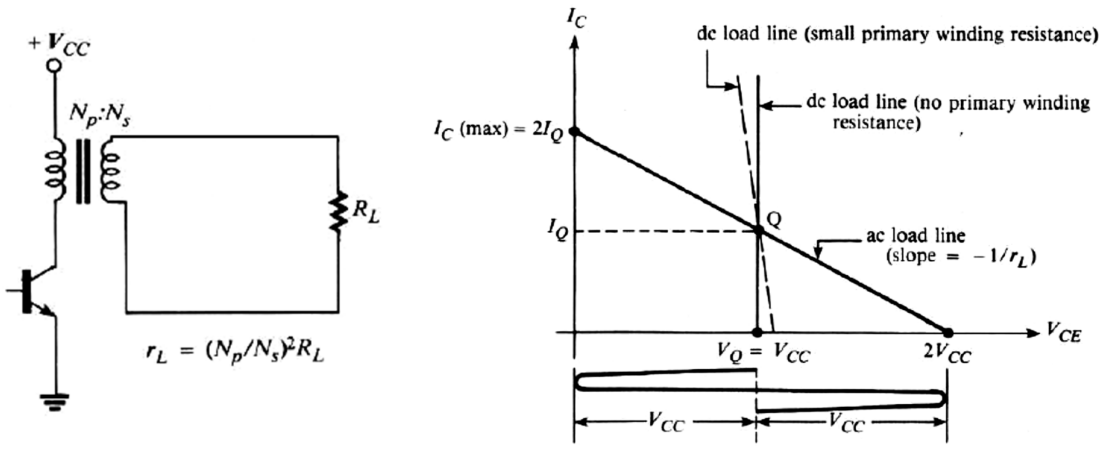


Fig. 3-6

The ac load line intersects the I_C-axis in Fig. 3-6 at I_C(max). There is no theoretical limit to the value that I_C may have, since there is no limiting resistance in the collector circuit. However, in practice, I_C must not exceed the maximum permissible collector current for the transistor and it must not be so great that the magnetic flux of the transformer saturates. When the transformer saturates, it can no longer induce current in the secondary winding and signal distortion results. When I_Q is set for maximum signal swing (so that $V_{CE}(\text{max}) = 2V_{CC}$), I_Q is one-half I_C(max); that is, $I_C(\text{max}) = 2I_Q$, as shown in Fig. 3-6. Thus, the maximum values of the peak primary voltage and peak primary current

are V_{CC} and I_Q, respectively. Since the ac output can vary through this range, below and above the quiescent point, the amplifier is of the class-A type.

Unlike the case of the capacitor-coupled or series-fed amplifier, the collector voltage can exceed the supply voltage. A transistor having a collector breakdown voltage equal to at least twice the supply voltage should be used in this application.

The ac power delivered to load resistance R_L in Fig. 3-6 is

$$P_L = \frac{V_s^2}{2R_L} = \frac{V_{PL}^2}{2R_L},$$

where $V_s = V_{PL}$ is the peak value of the secondary, or load, voltage. The average power from the dc supply is

$$P_S = V_{CC} I_Q.$$

Therefore, the efficiency is

$$\eta = \frac{P_L}{P_S} = \frac{V_{PL}^2}{2R_L V_{CC} I_Q} \qquad [3\text{-}11]$$

Under maximum signal conditions, the peak primary voltage is V_{CC} volts, so the peak load voltage is

$$V_{PL} = (N_s/N_p)V_{CC}.$$

Also, since the slope of the ac load line is $-1/r_L$, we have

$$\frac{|\Delta I_C|}{|\Delta V_{CE}|} = \frac{1}{r_L} = \frac{I_Q}{V_Q} \Rightarrow$$

$$I_Q = \frac{V_Q}{r_L} = \frac{V_{CC}}{(N_p/N_s)^2 R_L}.$$

Substituting the maximum values of V_{PL} and I_Q into Eqn. [3-11], we find the maximum possible efficiency of the transformer-coupled class-A amplifier:

$$\eta(\max) = \frac{(N_s/N_p)^2 V_{CC}^2}{(2R_L V_{CC}) \frac{V_{CC}}{(N_p/N_s)^2 R_L}} = 0.5$$

The maximum efficiency is twice that of the series-fed class-A amplifier and six times that of the capacitor-coupled class-A amplifier. This improvement in efficiency is attributable to the absence of external collector resistance that would otherwise consume dc power. The collector efficiency of the transformer-coupled class-A amplifier is the same as the overall amplifier efficiency, because the average power from the dc supply is the same as the collector dissipation:

$$P_S = V_{CC} I_Q = V_Q I_Q = P_C.$$

In practice, a full output voltage swing of $2V_{CC}$ volts cannot be achieved in a power transistor. The device is prevented from cutting off entirely by virtue of a relatively large leakage current, and it cannot be driven all the way into saturation ($I_C = I_C(\max)$) without creating excessive distortion.

Exercise 3-3:

The transistor in the power amplifier shown in Fig. 3-7(a) has the output characteristics shown in Fig. 3-7(b). Assume that the transformer has zero resistance.

(a) Construct the (ideal) dc and ac load lines necessary to achieve maximum output voltage swing. What quiescent values of collector and base current are necessary to realize the ac load line?

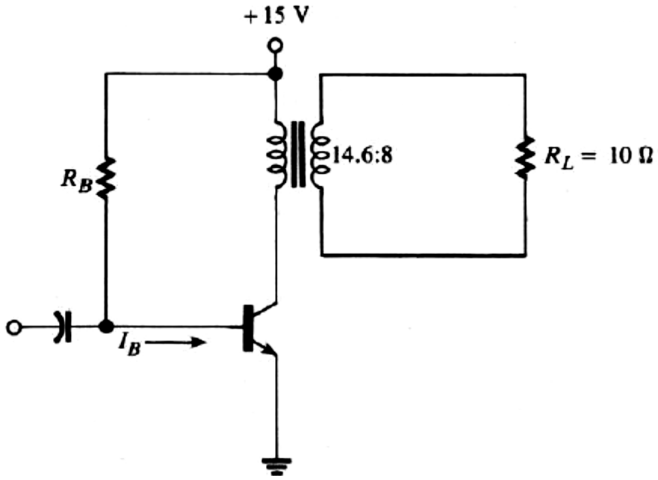
(b) What is the smallest value of $I_C(\max)$ for which the transistor should be rated?

(c) What is the maximum peak-to-peak collector voltage, and what peak-to-peak base current is required to achieve it? Assume that the base current cannot go negative and that, to minimize distortion, the collector should not be driven below 2.5 V in the saturation region.

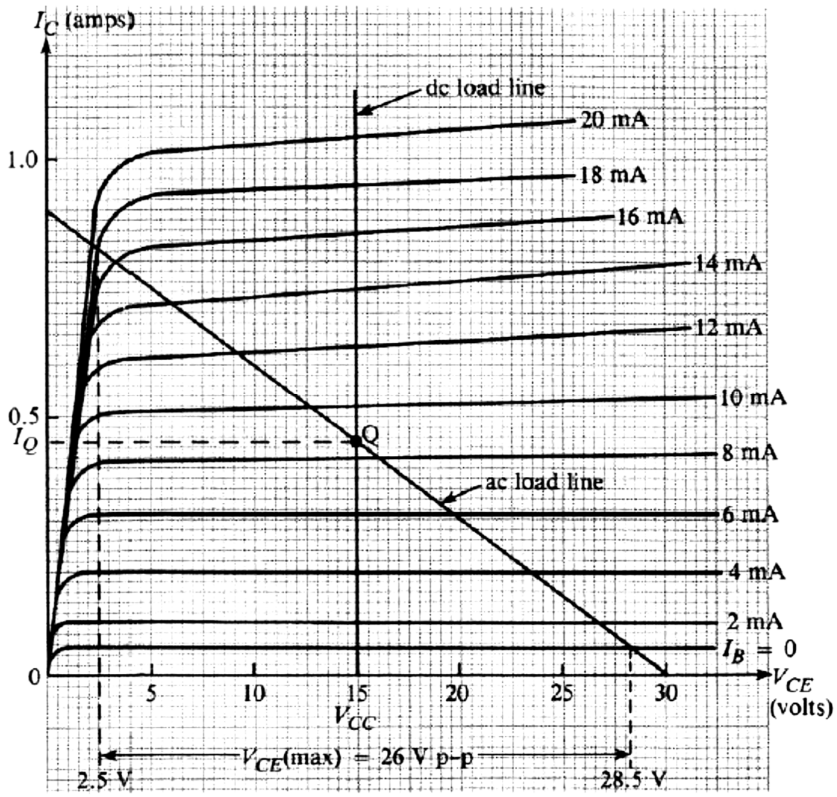
(d) Find the average power delivered to the load under the maximum signal conditions of part (c).

(e) Find the power dissipated in the transistor under no-signal conditions (standby).

(f) Find the efficiency.



(a)



(b)

Fig. 3-7

The Solution to Exercise 3-3:

(a) The vertical dc load line intersects the V_{CE}-axis at V_{CC} = 15 V, as shown in Fig. 3-7(b). To find the slope of the ac load line, we must find r_L. From Eqn. [3-10], $r_L = (N_p/N_s)^2 R_L = (14.6/8)^2(10) = 33.3\ \Omega$.
Thus, the slope of the ac load line is $-1/r_L = -1/33.3 = -0.03$ A/V. To achieve the ideal maximum output swing, we want the ac load line to intercept them V_{CE}-axis at $2V_{CC}$ = 30 V. Since the slope of that line has magnitude 0.03, it will intercept the I_C-axis at I_C = (0.03) (30) = 0.9 A. The ac load line is then drawn between the two intercepts (0 A, 30 V) and (0.9 A, 0 V), as shown in Fig. 3-7(b).
The ac load line intersects the dc load line at the Q-point. The quiescent collector current at that point is seen to be I_Q = 0.45 A. The corresponding base current is approximately halfway between I_B = 8 mA and I_B = 10 mA, so the quiescent base current must be 9 mA.

(b) The maximum collector current is I_C(max) = 0.9 A, at the intercept of the ac load line on the I_C-axis. Actually, we will not operate the transistor that far into saturation, since we do not allow V_{CE} to fall below 2.5 V. However, a maximum rating of 0.9 A (or 1 A) will provide us with a margin of safety.

(c) The maximum value of V_{CE} occurs on the ac load line at the point where I_B = 0. As shown in Fig. 3-7(b), this value is 28.5 V. Since the minimum permissible value of V_{CE} is 2.5 V, the maximum peak-to-peak voltage swing is 28.5 − 2.5 = 26 Vp-p. As can be seen on the characteristic curves, the base current must vary from I_B = 0 to I_B = 18 mA, or 18 mA peak-to-peak, to achieve that voltage swing.

(d) The peak primary voltage in the transformer is (l/2) (26) = 13 V. Therefore the peak secondary, or load voltage is $V_{PL} = (N_s/N_p)\ V_{P(\text{primary})}$ = (8/14.6) (13) = 7.12 V. The average load power is then
$P_L = \frac{V_{PL}^2}{2R_L} = \frac{(7.12)^2}{20} = 2.53$ W.

(e) The standby power dissipation is $P_d = V_Q I_Q = V_{CC} I_Q$ = (15) (0.45) = 6.75 W.

(f) The standby power dissipation found in part (e) is the same as the average power supplied from the dc source, so
η = 2.53/6.75 = 0.375
Question: Why is this value less than the theoretical maximum of 0.5?

3.4 Class-B Power Amplifiers:

Transistor operation is said to be class B when output current varies during only one half-cycle of a sine-wave input. In other words, the transistor is in its active region, responding to signal input, only during a positive half-cycle or only during a negative half-cycle of the input. This operation is illustrated in Fig. 3-8. In practical amplifiers, two transistors are operated class B: one to amplify positive signal variations and the other to amplify negative signal variations. The amplifier output is the composite waveform obtained by combining the waveforms produced by each class-B transistor. An amplifier utilizing transistors that are operated class B is called a class-B amplifier.

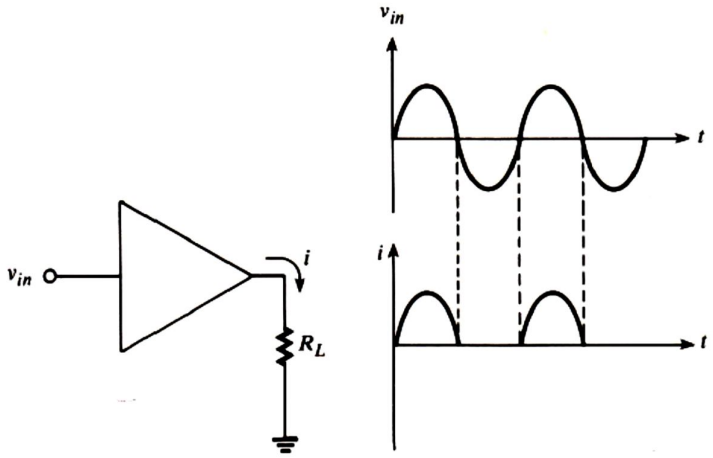


Fig. 3-8

3.4.1 Push-Pull Amplifiers:

A push-pull amplifier uses two output devices to drive a load. The name is derived from the fact that one device is primarily (or entirely) responsible for driving current through the load in one direction (pushing), while the other device drives current through the load in the opposite direction (pulling). The output devices are typically two transistors, each operated class B, one of which conducts only when the input is positive, and the other of which conducts only when the input is negative. This arrangement is called a class-B, push-pull amplifier and its principle is illustrated in Fig. 3-9.

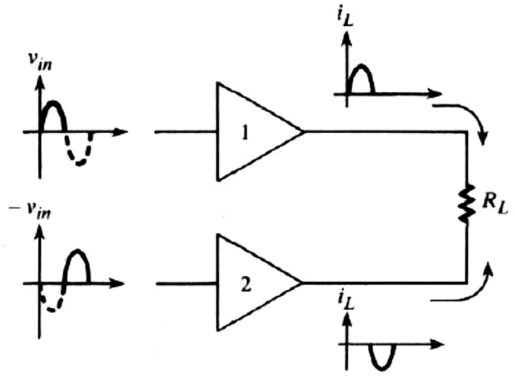


Fig. 3-9

In Fig. 3-9 that amplifying devices 1 and 2 are driven by equal-amplitude, out-of-phase input signals. The signals are identical except for phase. Here we assume that each device conducts only when its input is positive and is cut off when its input is negative. The net effect is that device 1 produces load current when the input is positive and device 2 produces load current, in the opposite direction, when the input is negative. An example of a device that has the property that it produces output (collector) current only when its input (base-to-emitter) voltage is positive is an NPN transistor having no base biasing circuitry, that is, one that is biased at cutoff. As we shall see, NPN transistors can be used as the output amplifying devices in push-pull amplifiers. However, the circuitry must be somewhat more elaborate than that diagrammed in Fig. 3-9, since we must make provisions for load current of low through a complete circuit, regardless of current direction. Obviously, when amplifying devise 1 in Fig. 3-9 is cut off, it cannot conduct current produced by device 2, and vice versa.

3.4.2 Push-Pull Amplifiers with Output Transformers:

Fig. 3-10 shows a push-pull arrangement that permits current to flow in both directions through a load even though one or the other of the amplifying devices (NPN transistors) is always cut off. The output transformer shown in the figure is the key component. The primary winding is connected between the transistor collectors and that its center tap is connected to the dc supply, V_{CC}. The center tap is simply an electrical connection made at the center of the winding, so there are an equal number of turns between each end of the winding and the center tap. The figure does not show the push-pull driver circuitry, which must produce out-of-phase signals on the bases of Q_1 and Q_2.

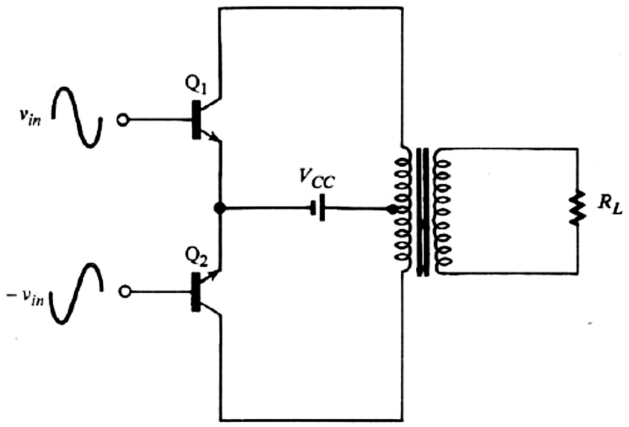
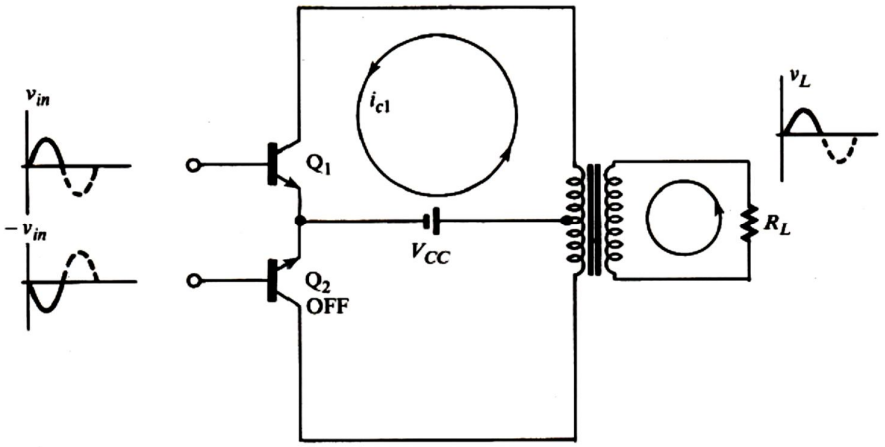


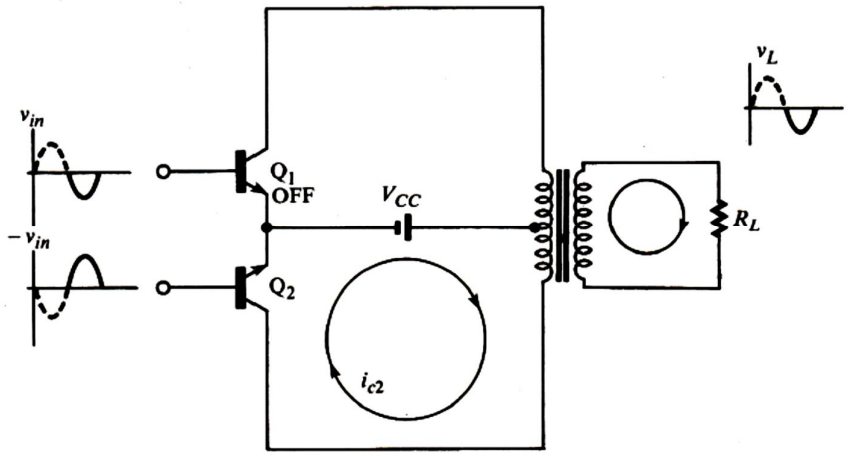
Fig. 3-10

Fig. 3.11 shows how current flows through the amplifier during a positive half-cycle of input and during a negative half-cycle of input. In Fig. 3.11(a), the input to Q_1 is the positive half-cycle of the signal, and since the input to Q_2 is out-of-phase with that to Q_1, Q_2 is driven by a negative half-cycle. Neither class-B transistor is biased. Consequently, the positive base voltage on Q_1 causes it to turn on and conduct current in the counterclockwise path shown. The negative base voltage on Q_2 keeps that transistor cut off. Current flowing in the upper half of the transformer's primary induces current in the secondary, and current flows through the load.

In Fig. 3.11(b), the input signal on the base of Q_1 has gone negative, so its inverse on the base of Q_2 is positive. Therefore, Q_2 conducts current in the clockwise path shown, and Q_1 is cut off. Current induced in the secondary winding is in the direction opposite that shown in Fig. 3-11(a). The upshot is that current flows through the load in one direction when the input signal is positive and in the opposite direction when the input signal is negative, just as it should in an ac amplifier.



(a)



(b)

Fig. 3-11

Fig. 3-12 displays current flow in the push-pull amplifier in the form of a timing diagram. Here the complete current waveforms are shown over two full cycles of input. For purposes of this illustration, counterclockwise current (in Fig. 3-11) is arbitrarily assumed to be positive and clockwise current is therefore negative. As far as the load is concerned, current flows during the full 360º of input signal. Fig. 3-12(e) shows that the current i_S from the power supply varies from 0 to the peak value I_P every half-cycle. Because the current variation is so large, the power supply used in a push-pull amplifier must be particularly well regulated-that is, it must maintain a constant voltage, independent of current demand.

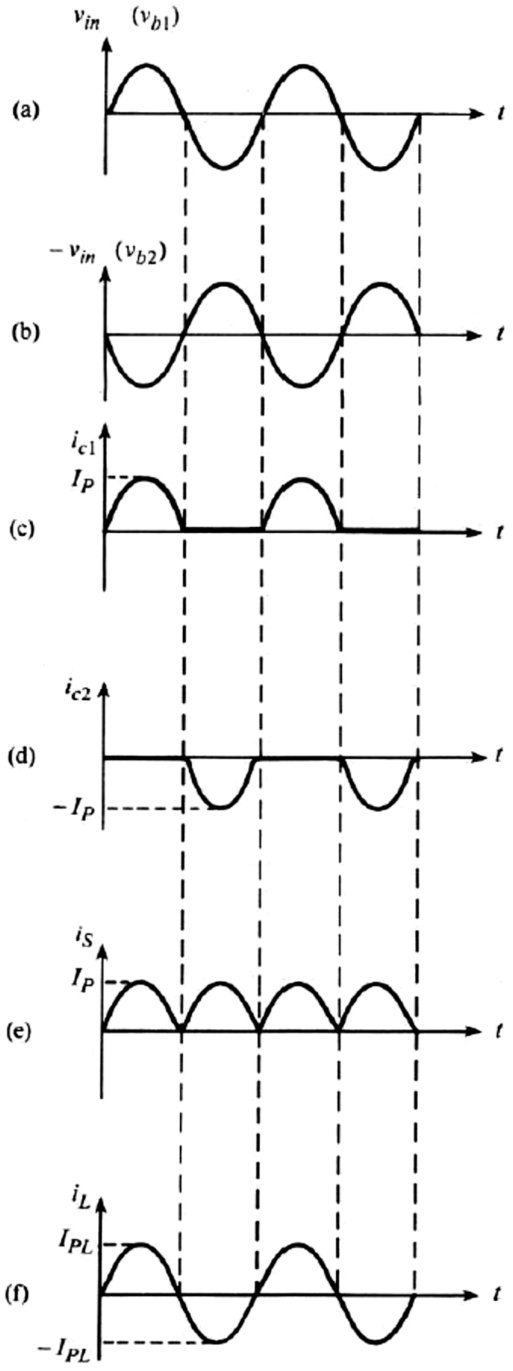


Fig. 3-12

3.4.3 Class-B Efficiency:

The principal advantage of using a class-B power amplifier is that it is possible to achieve an efficiency greater than that attainable in a class-A amplifier. The improvement in efficiency stems from the fact that no power is dissipated in a transistor during the time intervals that it is cut off. Also, like the transformer-coupled class-A amplifier, there is no external collector resistance that would otherwise consume power.

We will derive an expression for the maximum efficiency of a class-B push-pull power amplifier assuming ideal conditions: perfectly matched transistors and zero resistance in the transformer windings. The current supplied by each transistor is a

half-wave-rectified waveform, as shown in Fig. 3-12. Let I_P represent the peak value of each. Then the peak value of the current in the secondary winding, which is the same as the peak load current, is

$$I_{PL} = (N_p/N_s)I_P$$

where N_p/N_s, is the turns ratio between one-half the primary winding and the secondary winding ($N_p = N_{p(\text{total})}/2$). Note that only those primary turns between one end of the winding and its center tap are used to induce current in the secondary. Similarly, the peak value of the load voltage is

$$V_{PL} = (N_s/N_p)V_P$$

where V_P is the peak value of the primary (collector) voltage. Since the load voltage and load current are sinusoidal, the average power delivered to the load is, from Eqn. [3-4],

$$P_L = \frac{V_{PL}I_{PL}}{2} = \frac{(N_s/N_p)V_P(N_p/N_s)I_P}{2} = \frac{V_P I_P}{2}.$$

As shown in Fig. 3-12(e), the power-supply current is a full-wave-rectified waveform having peak value I_P. The dc, or average, value of such a waveform is known to be $2I_p/\pi$. Therefore, the average power delivered to the circuit by the dc supply is

$$P_S = \frac{2I_P V_{CC}}{\pi}.$$

The efficiency is then

$$\eta = \frac{P_L}{P_S} = \frac{V_P I_P/2}{2I_P V_{CC}/\pi} = \frac{\pi V_P}{4V_{CC}} \qquad [3\text{-}12]$$

Under maximum signal conditions, $V_P = V_{CC}$, and Eqn. [3-12] becomes

$$\eta(\text{max}) = \frac{\pi}{4} = 0.785$$

This equation shows that a class-B push-pull amplifier can be operated with a much higher efficiency than the class-A amplifiers studied earlier. Furthermore, unlike the case of class-A amplifiers, the power dissipated in the transistors is 0 under standby (zero signal) conditions, because both transistors are cut off. A general expression for the total power dissipated in the transistors can be obtained by realizing that it equals the difference between the total power supplied by the dc source and the total power delivered to the load:

$$P_d = P_S - P_L = \frac{2I_P V_{CC}}{\pi} - \frac{V_P I_P}{2}.$$

Using calculus, it can be shown that P_d is maximum when $V_P = 2V_{CC}/\pi = 0.636V_{CC}$. We conclude that maximum transistor dissipation does not occur when maximum load power is delivered ($V_P = V_{CC}$), but at the intermediate level $V_P = 0.636V_{CC}$.

Exercise 3-4:

The push-pull amplifier in Fig. 3-10 has V_{CC} = 20 V and R_L = 10 Ω. The total number of turns on the primary winding is 100 and the secondary winding has 50 turns. Assume that the transformer has zero resistance.

(a) Find the maximum power that can be delivered to the load.
(b) Find the power dissipated in each transistor when maximum power is delivered to the load.
(c) Find the power delivered to the load and the power dissipated in each transistor when transistor power dissipation is maximum.

[Answers: (a) 20 W, (b) 2.73 W, (c) 8.09 W, 4.05 W]

3.4.4 Push-Pull Drivers:

The push-pull amplifier must be driven by out-of-phase input signals. Fig. 3-13 shows how a transformer can be used to provide the required drive signals. Here, the secondary winding has a grounded center tap that effectively splits the secondary voltage into two out-of-phase signals, each having one-half the peak value of the total secondary voltage. The input signal is applied across the primary winding and a voltage is developed across secondary terminals A-B, in the usual transformer fashion.

To understand the phase splitting action, consider the instant at which the voltage across A-B is +6 V, as shown in the figure. Then, since the center point is at ground, the voltage from A to ground must be +3 V and that from B to ground must be −3V:

$V_{AB} = V_A - V_B = 3 - (-3) = +6$ V.

The same logic applied at every instant throughout a complete cycle shows that v_B with respect to ground is always the negative of v_A with respect to ground; in other words, v_A and v_B are equal-amplitude, out-of-phase driver signals, as required.

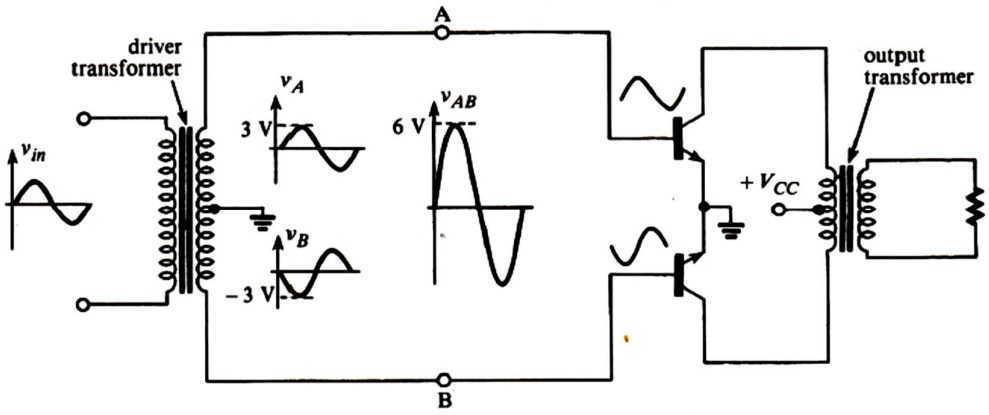
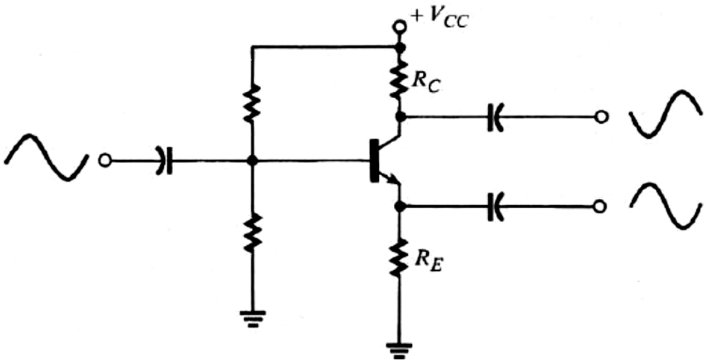


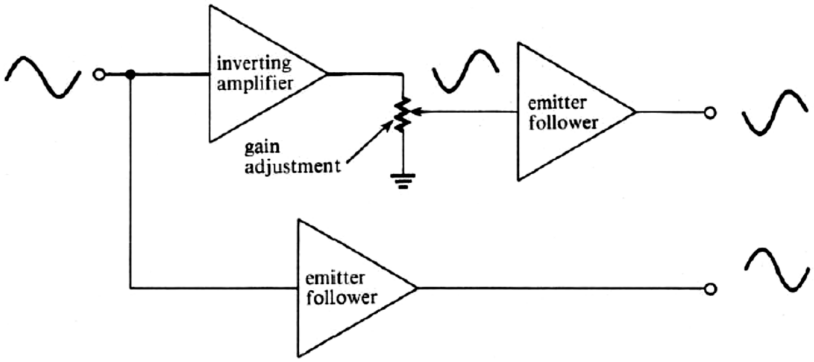
Fig. 3-13

A specially designed amplifier, called a phase-splitter, can be used instead of a driver transformer to produce equal-amplitude, out-of-phase drive signals. Fig. 3-14 shows two possible designs. Fig. 3-13(a) is a conventional amplifier circuit with outputs taken at the collector and at the emitter. The collector output is out of phase with the input and the emitter output is in phase with the input, so the two outputs are out of phase with each other. With no load connected to either output, the output signals will have approximately equal amplitudes if $R_C = R_E$. However, the output impedance at the collector is significantly greater than that at the emitter, so when loads are connected, each output will be affected differently.

As a consequence, the signal amplitudes will no longer be equal, and gain adjustments will be required. Furthermore, the nonlinear nature of the large signal load (the output transistors) means that the gain of the collector output may vary appreciably with signal level. Intolerable distortion can be created as a result. A better way to drive the output transistors is from two low-impedance signal sources, as shown in Fig. 3-14(b). Here, the output from an inverting amplifier is buffered by an emitter-follower stage, as is the original signal.



(a)



(b)

Fig. 3-14

3.4.5 Distortion in Push-Pull Amplifiers:

***Cancellation of Even Harmonics*:**

Recall that push-pull operation effectively produces in a load a waveform proportional to the difference between two input signals. Under normal operation, the signals are out of phase, so their waveform is reproduced in the load. If the signals were in phase, cancellation would occur. It can be shown that a half-wave-rectified sine wave contains only the fundamental and all even harmonics. Fig. 3-15(a) shows the two out-of-phase half-wave-rectified sine waves that drive the load, and Fig. 3-15(b) shows the fundamental and second-harmonic components of each. The fundamental components are out of phase. Therefore, the fundamental component is reproduced in the load, as we have already seen (Fig. 3-12). However, the second-harmonic components are in phase, and therefore cancel in the load. Although not shown in Fig. 3-15(b), the fourth and all other even harmonics are also in phase and therefore also cancel. Our conclusion is an important property of push-pull amplifies: even harmonics are cancelled in push-pull operation.

The cancellation of even harmonics is an important factor in reducing distortion in push-pull amplifiers. However, perfect cancellation would occur only if the two sides were perfectly matched and perfectly balanced: identical transistors, identical drivers, and a perfectly center-tapped transformer. Of course, this is not the case in practice, but even imperfect push-pull operation reduces even harmonic distortion. Odd harmonics are out of phase, so cancellation of those components does not occur.

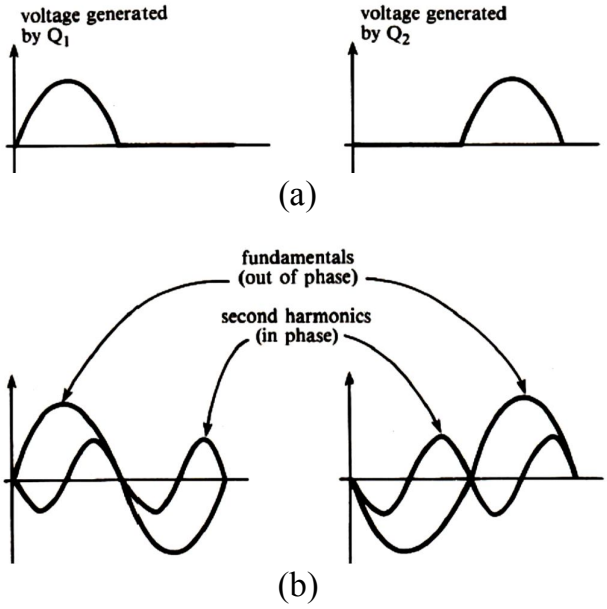


Fig. 3-15

Crossover Distortion:

A forward-biasing voltage applied across a PN junction must be raised to a certain level (about 0.7 V for silicon) before the junction will conduct any significant current. Similarly, the voltage across the base-emitter junction of a transistor must reach that level before any appreciable base current, and hence collector current, can flow. As a consequence, the drive signal applied to a class-B transistor must reach a certain minimum level before its collector current is properly in the active region. This fact is the principal source of distortion in a class-B, push-pull amplifier, as illustrated in Fig. 3-16.

Fig. 3-16(a) shows that the initial rise of collector current in a class-B transistor lags the initial rise of input voltage, for the reason we have described. Also, collector current prematurely drops to 0 when the input voltage approaches 0. Fig. 3-16(b) shows the voltage wave form that is produced in the load of a push-pull amplifier when the distortion generated during each half-cycle by each class-B transistor is combined. This distortion is called ***crossover distortion***, because it occurs where the composite waveform crosses the zero voltage axes. Clearly, the effect of crossover distortion becomes more serious as the signal level becomes smaller.

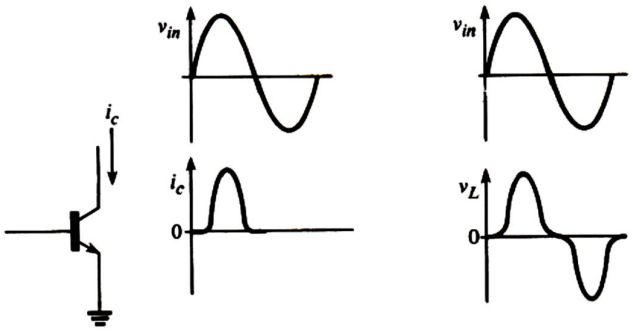
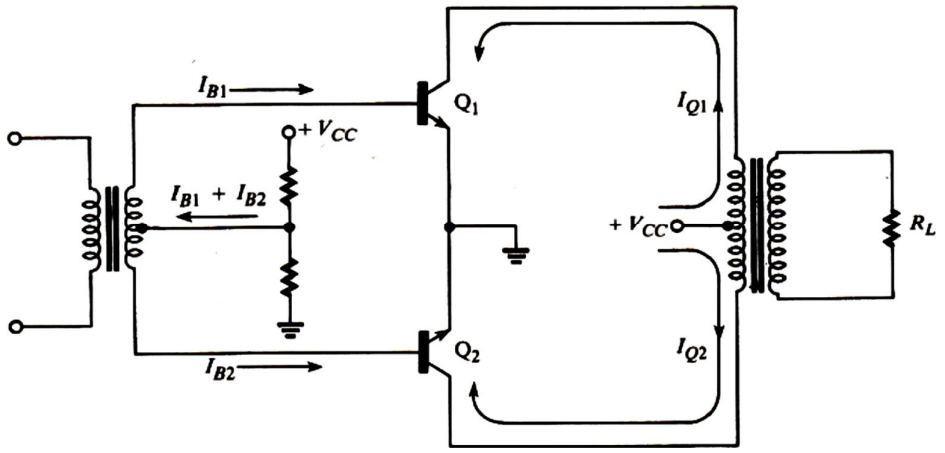


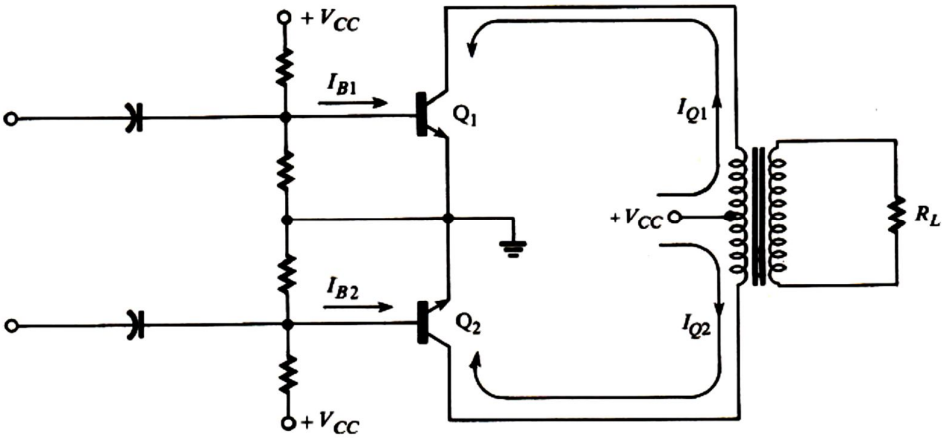
Fig. 3-16

2.5 Class-AB Power Amplifiers:

Crossover distortion can be reduced or eliminated in a push-pull amplifier by biasing each transistor slightly into conduction. When a small forward-biasing voltage is applied across each base-emitter junction, and a small base current flows under no-signal conditions, it is not necessary for the base drive signal to overcome the built-in junction potential before active operation can occur. A simple voltage-divider bias network can be connected across each base for this purpose, as shown in Fig. 3-17. Fig. 3-17(a) shows how two resistors can provide bias for both transistors when a driver transformer is used. Fig. 3-17(b) shows the use of two voltage dividers when the drive signals are capacitor coupled. Typically, the base-emitter junctions are biased at about 0.5 V for silicon transistors, or so that the collector current under no-signal conditions is about 1% of its peak signal value.



(a)



(b)

Fig. 3-17

When a transistor is biased slightly into conduction, output current will flow during more than one-half cycle of a sine-wave input, as illustrated in Fig. 3-18. As can be seen in the figure, conduction occurs for more than one-half but less than a full cycle of input. This operation, which is neither class A nor class B, is called class-AB operation.

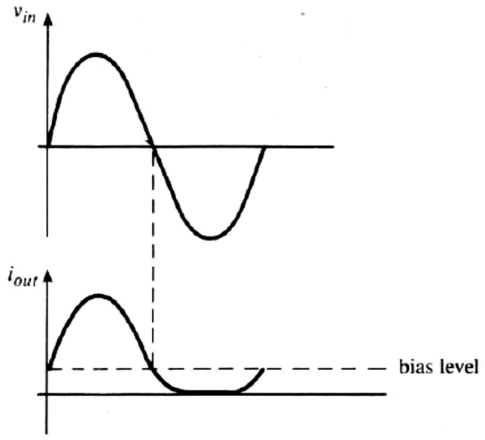


Fig. 3-18

While class-AB operation reduces crossover distortion in a push-pull amplifier, it has the disadvantage of reducing amplifier efficiency. The fact that bias current is always present means that there is continuous power dissipation in both transistors, including the time intervals during which one of the transistors would be cut off if the operation were class B. The extent to which efficiency is reduced depends directly on how heavily the transistors are biased, and the maximum achievable efficiency is somewhere between that which can be obtained in class-A operation (0.5) and that attainable in class-B operation (0.785).

In Fig. 3-17, the quiescent collector currents I_{Q1} and I_{Q2} flow in opposite directions though the primary of the transformer. Thus, the magnetic flux created in the transformer by one dc current opposes that created by the other, and the net flux is 0. This is an advantageous situation, in comparison with the class-A transformer-coupled amplifier, because it means that transformer current can swing positive and negative through a maximum range. If the transformer flux had a bias component, the signal swing would be limited in one direction by the onset of magnetic saturation.

3.6 Transformerless Push-Pull Amplifiers:

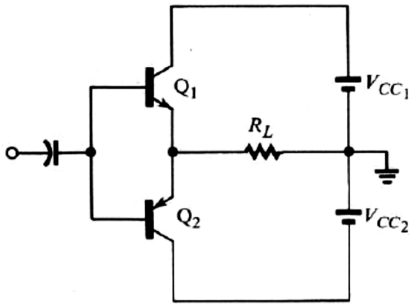
The principal disadvantage of the push-pull amplifier circuits we have discussed so far is the cost and bulk of their output transformers. High-power amplifiers in particular are encumbered by the need for very large transformers capable of conducting large currents without saturating.

3.6.1 Complementary Push-Pull Amplifiers:

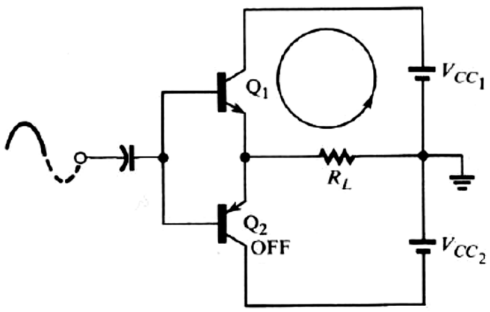
Fig. 3-19(a) shows a popular design using complementary (PNP and NPN) output transistors to eliminate the need for an output transformer in push-pull operation. This design also eliminates the need for a driver transformer or any other drive circuitry producing out-of-phase signals.

Fig. 3-19(b) shows that current flows in a counterclockwise path through the load when the input signal on the base of NPN transistor Q_1 is positive. The positive inputs, simultaneously, appears on the base of PNP transistor Q_2 and keeps it cut off. When the input is negative, Q_1 is cut off and Q_2 conducts current through the load in the opposite direction, as shown in Fig. 3-19(c).

Each transistor in Fig. 3-19 drives the load in an emitter-follower configuration. The advantageous consequence is that low-impedance loads can be driven from a low impedance source. Also, the large negative feedback that is inherent in emitter-follower operation reduces the problem of output distortion. However, as is the case in all emitter followers, voltage gains greater than unity cannot be realized. The maximum positive voltage swing is V_{CC1} and the maximum negative swing is V_{CC2}. Normally, $|V_{CC1}| = |V_{CC2}| = |V_{CC}|$, so the maximum peak-to-peak swing is $2V_{CC}$ volts. Since the voltage gain is near unity, the input must also swing through $2V_{CC}$ volts to realize maximum output swing. Under conditions of maximum swing, the cut-off transistor has a reverie-biasing collector-to-base voltage of $2V_{CC}$ volts, so each transistor must have a rated breakdown voltage of at least that amount.



(a)



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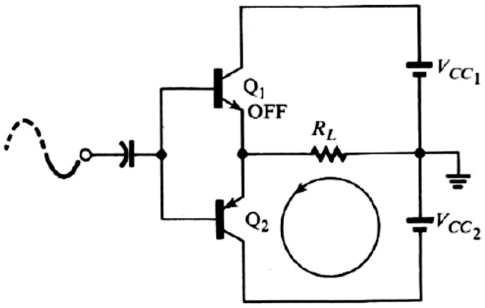
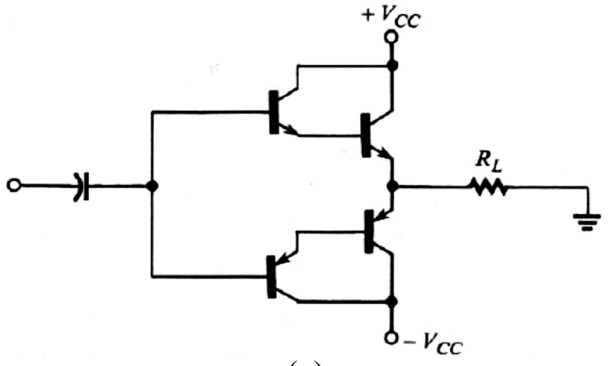


(c)

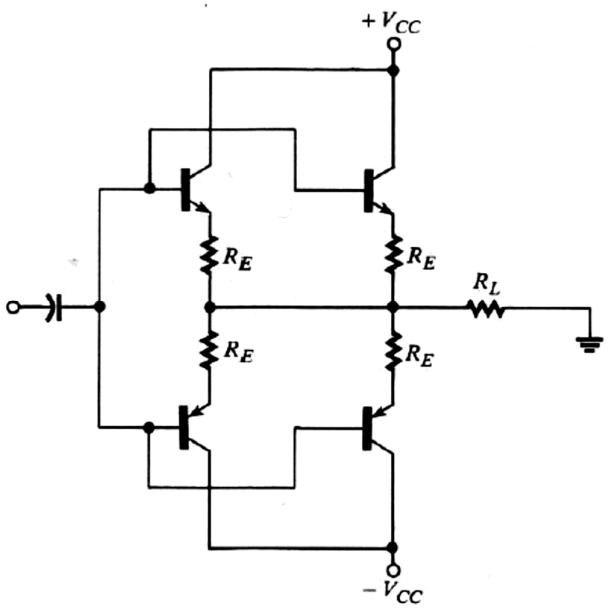
Fig. 3-19

Fig. 3.20 shows two variations on the basic complementary, push-pull amplifier. In Fig. 3.20(a), the transistors are replaced by emitter-follower Darlington pairs. Since power transistors tend to have low betas, particularly at high current levels, the Darlington pair improves the drive capabilities and the current gain of the amplifier. These devices are available in matched complementary sets with current ratings up to 20 amperes.

Fig. 3-20(b) shows how emitter-follower transistors can be operated in parallel to increase the overall current-handling capability of the amplifier. In this variation, the parallel transistors must be closely matched to prevent "current hogging", wherein one device carries most of the load, thus subverting the intention of load sharing. Small emitter resistors R_E shown in the figure introduce negative feedback and help prevent current hogging, at the expense of efficiency. Amplifiers capable of dissipating several hundred watts have been constructed using this arrangement.



(a)



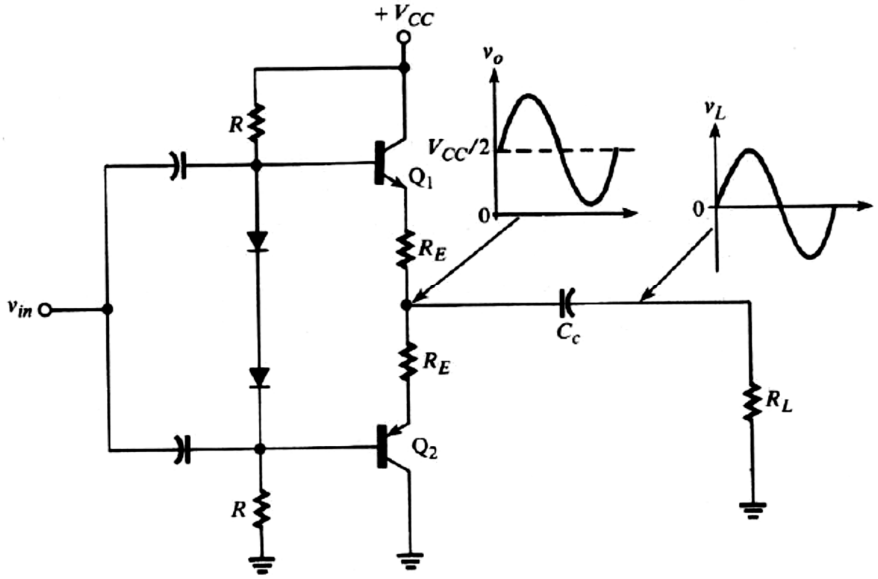
(b)

Fig. 3-20

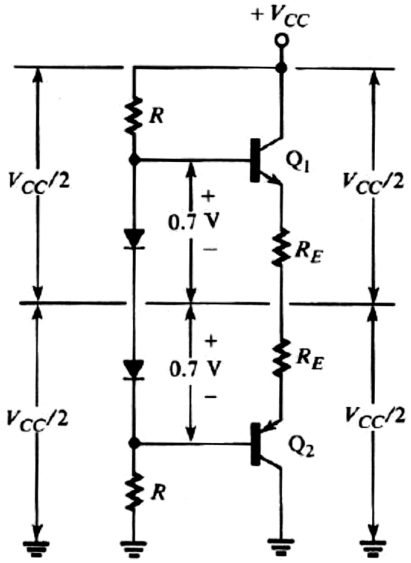
One disadvantage of the complementary push-pull amplifier is the need for two power supplies. Also, like the transformer-coupled push-pull amplifier, the complementary class-B amplifier produces crossover distortion in its output. Fig. 3-21(a) shows another version of the complementary amplifier that eliminates these problems and that incorporates some additional features.

The complementary amplifier in Fig. 3-21 can be operated with a single power supply because the output v_o, is biased at half the supply voltage and is capacitor-coupled to the load. The resistor-diode network connected across the transistor bases is used to bias each transistor near the threshold of conduction. Crossover distortion can be reduced or eliminated by inserting another resistor (not shown in the figure) in series with the diodes to bias the transistors further into AB-operation. Assuming that an components are perfectly matched, the supply voltage will divide equally across each half of the amplifier, as shown in Fig. 3.21(b). In practice, one of the resistors R can be made adjustable for balance purposes. Resistors R_E provide bias stability to prevent thermal runaway, but are made as small as possible since they adversely affect efficiency. Since each half of the

amplifier has $V_{CC}/2$ volts across it, the forward-biased diode drops appear across the base-emitter junctions with the proper polarity to bias each transistor towards conduction. The diodes are selected so that their characteristics track the base emitter junctions under temperature changes and thus ensure bias stability. The diodes are typically mounted on the same heat sinks as the transistors so that both change temperature in the same way.



(a)



(b)

Fig. 3-21

In ac operation, when input v_1 is positive and Q_1 is conducting, current is drawn from the power supply and flows through Q_1 to the load. When Q_1 is cut off by a negative input, no current can flow from the supply. At those times, Q_2 is conducting and capacitor C_c discharges through that transistor. Thus, current flows from the load through C_c, and through Q_2 to ground whenever the input is negative.

The R_LC_c time constant must be much greater than the period of the lowest signal frequency. The lower cutoff frequency due to C_c is given by

$$f_L(C_c) = \frac{1}{2\pi(R_L+R_E)C_c} \quad [3\text{-}13]$$

The peak load current is the peak input voltage V_P divided by $R_L + R_E$:

$$I_{PL} = \frac{V_P}{R_L+R_E}$$

Therefore, the average ac power delivered to the load is

$$P_L = \frac{I_{PL}^2 R_L}{2} = \frac{V_P^2 R_L}{2(R_L+R_E)^2}$$

Since current is drawn from the power supply only during positive half-cycles of input, the supply-current waveform is half-wave rectified, with peak value $V_P/(R_L + R_E)$ amperes. Therefore, the average value of the supply current is

$$I_S(\text{avg}) = \frac{V_P}{\pi(R_L+R_E)}$$

and the average power from the supply is

$$P_S = V_{CC} I_S(\text{avg}) = \frac{V_{CC}V_P}{\pi(R_L+R_E)}$$

We find the efficiency to be

$$\eta = \frac{P_L}{P_S} = \frac{\pi}{2}\left(\frac{R_L}{R_L+R_E}\right)\left(\frac{V_P}{V_{CC}}\right) \quad [3\text{-}14]$$

The efficiency is maximum when the peak voltage V_P has its maximum possible value, $V_{CC}/2$. In that case,

$$\eta(\text{max}) = \frac{\pi}{2}\left(\frac{R_L}{R_L+R_E}\right)\left(\frac{V_{CC}/2}{V_{CC}}\right) = \frac{\pi}{4}\left(\frac{R_L}{R_L+R_E}\right)$$

The last two equations show that efficiency decreases, as expected, when R_E is increased. If R_E = 0, then the maximum possible efficiency becomes $\eta(\text{max}) = \pi/4 = 0.785$, the theoretical maximum for a class-B amplifier.

3.6.2 Quasi-Complementary Push-Pull Amplifiers:

Modern semiconductor technology is such that NPN transistors are generally superior to PNP types. Fig. 3-22 shows a popular push-pull amplifier design that uses NPN transistors for both output devices. This design is called quasi-complementary because transistors Q_3 and Q_4 together perform the same function as the PNP transistor in a complementary push-pull amplifier.

When the input signal is positive, PNP transistor Q_3 is cut off, so NPN transistor Q_4 receives no base current and is also cut off. When the input is negative, Q_3 conducts and supplies base current to Q_4, which can then conduct load current. Transistors Q_1 and Q_2, form an NPN Darlington pair, so Q_1 and Q_2 provide emitter-follower action to the load when the input is positive, and Q_3 and Q_4 perform that function when the input is negative. The entire configuration thus performs push-pull operation in the same manner as the complementary push-pull amplifier. The current gain of the Q_3Q_4 combination is

$$\frac{I_E}{I_B} = \beta_3\beta_4 + (1 + \beta_3)$$

This gain is very nearly that of a Darlington pair. Transistors Q_1 and Q_2 are connected as a Darlington pair to ensure that both sides of the amplifier have similar gain.

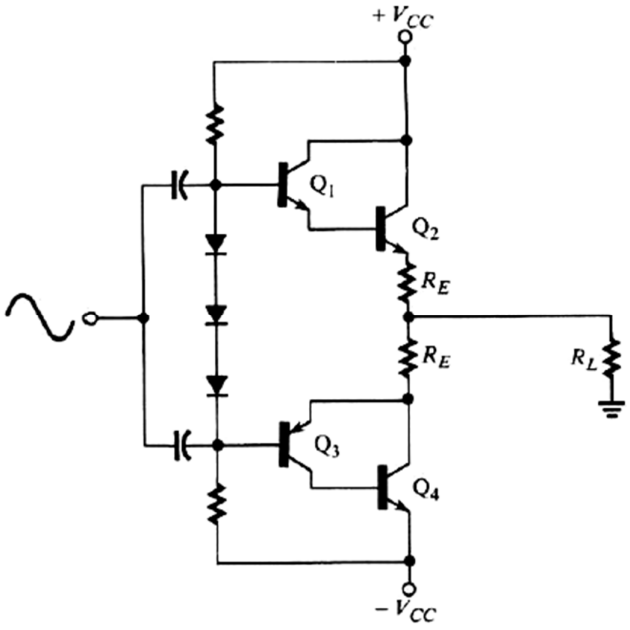


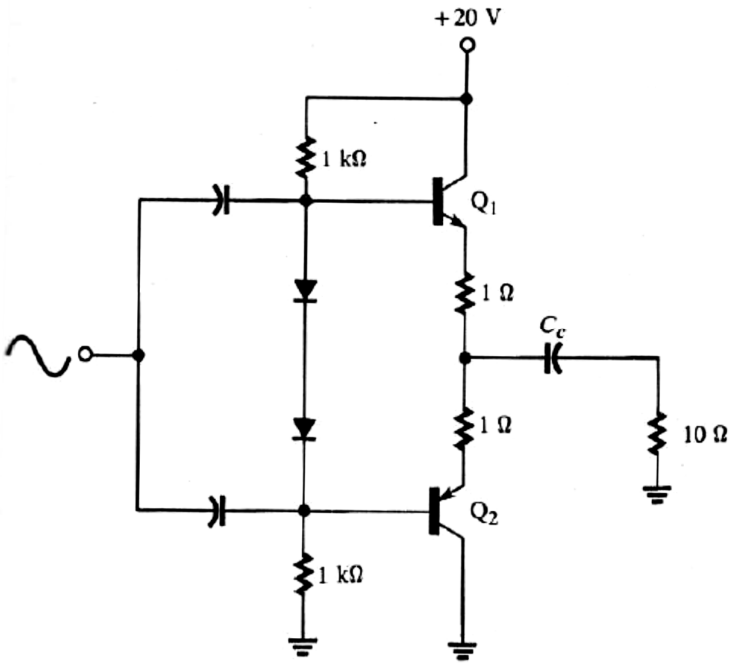
Fig. 3-22

Exercise 3-5:

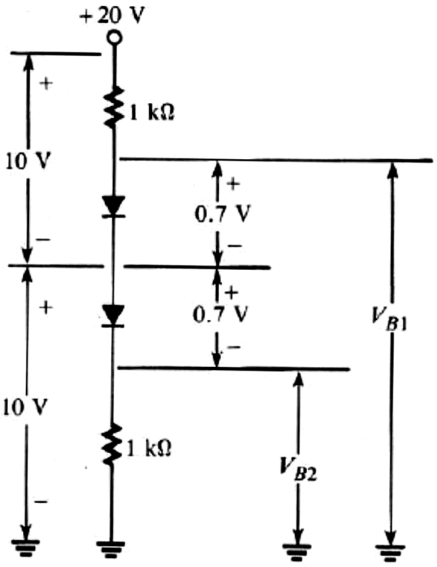
Assuming that all components in Fig. 3-23(a) are perfectly matched, find

(a) the base-to-ground voltages V_{B1} and V_{B2} of each transistor,
(b) the power delivered to the load under maximum signal conditions,
(c) the efficiency under maximum signal conditions, and
(d) the value of capacitor C_c if the amplifier is to be used at signal frequencies down to 20 Hz.

[Answers: (a) 10.7 V, 9.3 V, Fig. 3-23(b), (b) 4.132 W, (c) 0.714, (d) 723 μF]



(a)



(b)

Fig. 3-23

3.7 Class-C Power Amplifiers:

A class-C amplifier is one whose output conducts load current during less than one-half cycle of an input sine wave. Fig. 3-24 shows a typical class-C current waveform, and it is apparent that the total angle during which current flows-is less than 180º. This angle is called the conduction angle, θ_c.

Of course, the output of a class-C amplifier is a highly distorted version of its input. It could not be used in an application requiring high fidelity, such as an audio amplifier. Class-C amplifiers are used primarily in high-power, high-frequency applications, such as radio-frequency transmitters. In these applications, the high-frequency pulses handled by the amplifier are not themselves the signal, but constitute what is called the carrier for the signal. The signal is transmitted by varying the amplitude of the carrier, using the process called, amplitude modulation (AM). The signal is ultimately recovered in a receiver by filtering out the carrier frequency. The principal advantage of a class-C amplifier is that it has a very high efficiency.

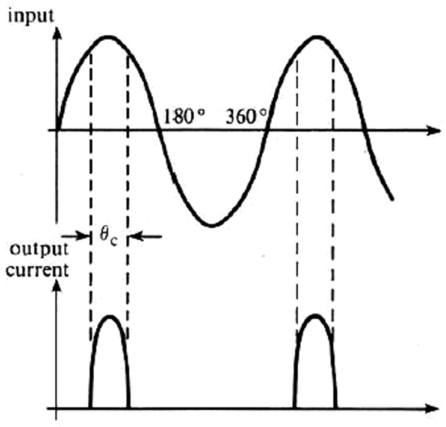


Fig. 3-24

Fig. 3-25 shows a simple class-C amplifier with a resistive load. The base of the NPN transistor is biased by a negative voltage, $-V_{BB}$, connected through a coil labeled RFC. The RFC is a radio-frequency choke whose inductance presents a high impedance to the high-frequency input and thereby prevents the dc source from shorting the ac input. In order for the transistor to begin conducting, the input must reach a level sufficient to overcome both the negative bias and the V_{BE} drop of about 0.7 V:

$$V_c = |V_{BB}| + 0.7$$

where V_c is the input voltage at which the transistor begins to conduct. As shown in the figure, the transistor is cut off until v_{in} reaches V_c, then it conducts, and then it cuts off again when v_{in} falls below V_c. Clearly, the more negative the value of V_{BB}, the shorter the conduction interval. In most class-C applications, the amplifier is designed so that the peak value of the input, V_P, is just sufficient to drive the transistor into saturation.

The conduction angle θ_c in Fig. 3-25 can be found from

$$\theta_c = 2 \arccos\left(\frac{V_c}{V_P}\right)$$

where V_P is the peak input voltage that drives the transistor to saturation. If the peak input only just reaches V_c, then $\theta_c = 2 \arccos(1) = 0º$. At the other extreme, if $V_{BB} = 0$, then $V_c = 0.7$, $(V_c/V_P) \approx 0$, and $\theta_c = 2 \arccos(0) = 180$ °, which corresponds to class-B operation.

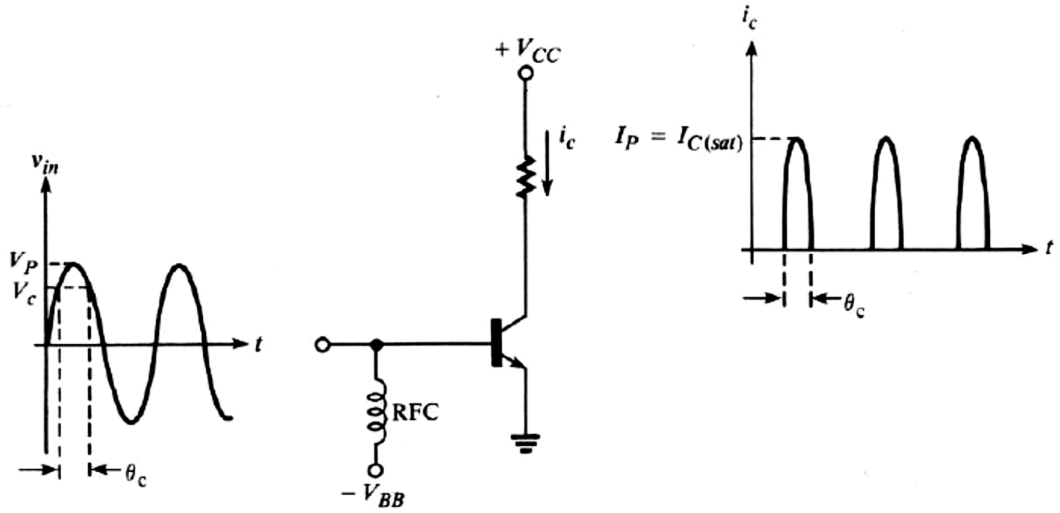


Fig. 3-25

Fig. 3-26 shows the class-C amplifier as it is normally operated, with an LC tank network in the collector circuit. The tank is a resonant network whose center frequency, assuming small coil resistance, is closely approximated by

$$f_o \approx \frac{1}{2\pi\sqrt{LC}}$$

The purpose of the tank is to produce the fundamental component of the pulsed, class-C waveform, which has the same frequency as v_{in}. The configuration is called a tuned amplifier, and the center frequency of the tank is set equal to (tuned to) the input frequency. There are several ways to view its behavior as an aid in understanding how it recovers the fundamental frequency. We may regard the tank as a highly selective (high-Q) filter that suppresses the harmonics in the class-C waveform and passes its fundamental. The voltage gain of the transistor equals the impedance in the collector circuit divided by the emitter resistance. Since the impedance of the tank is very large at its center frequency, the gain is correspondingly large at that frequency, while the impedance and the gain at harmonic frequencies are much smaller.

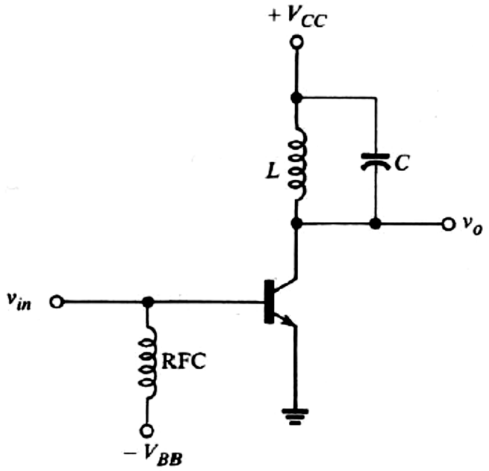


Fig. 3-26

The amplitude of the fundamental component of a class-C waveform depends on the conduction angle θ_c. The greater the conduction angle, the greater the ratio of the amplitude of the fundamental component to the amplitude of the total waveform. Let r_1 be the ratio of the peak value of the fundamental component to the peak value of the class-C waveform. The value of r_1 is closely approximated by

$$r_1 \approx (-3.54 + 4.1\,\theta_c - 0.0072\,\theta_c^2) \times 10^{-3}$$

where $0^\circ \le \theta_c \le 180^\circ$. The values of r_1 vary from 0 to 0.5 as θ_c varies from 0º to 180º.

Let r_0 be the ratio of the dc value of the class-C waveform to its peak value. The value of r_0 can be found from

$$r_0 = \frac{\text{dc value}}{\text{peak value}} = \frac{\theta_c}{\pi(180)}$$

where $0^\circ \le \theta_c \le 180^\circ$. The values of r_0 vary from 0 to $1/\pi$ as θ_c varies from 0º to 180º.

The efficiency of a class-C amplifier is large because very little power is dissipated when the transistor is cut off, and it is cut off during most of every full cycle of input. The output power at the fundamental frequency under maximum drive conditions is

$$P_o = \frac{(r_1 I_P)V_{CC}}{2}$$

where I_P is the peak output (collector) current. The average power supplied by the dc source is V_{CC} times the average current drawn from the source. Since current flows only when the transistor is co ducting, this current waveform is the same as the class-C collector-current waveform having peak value I_P. Therefore,

$$P_S = (r_0 I_P)V_{CC}$$

The efficiency is then

$$\eta_c = \frac{P_o}{P_S} = \frac{r_1 I_P V_{CC}}{2 r_0 I_P V_{CC}} = \frac{r_1}{2 r_0} \qquad [3\text{-}15]$$

Exercise 3-6:

A class-C amplifier has a base bias voltage of −5 V and V_{CC} = 30 V. It is determined that a peak input voltage of 9.8 V at 1 MHz is required to drive the transistor to its saturation current of 1.8 A.

(a) Find the conduction angle.
(b) Find the output power at 1 MHz.
(c) Find the efficiency.
(d) If an LC tank having C = 200pF is connected in the collector circuit, find the inductance necessary to tune the amplifier.

[Answers: (a) 108.9º, (b) 9.64 W, (c) 0.925, (d) 0.127 mH]

20 MHz. For higher frequencies, the crystal must be operated in the overtone mode. Overtones are approximate integer multiples of the fundamental frequency. The overtone frequencies are usually, but not always, odd multiples (3, 5, 7, …) of the fundamental. Many crystal oscillators are available in integrated circuit packages.

Exercise 4-4:

A crystal has these values: L_s = 3 H, C_s = 0.05 pF, R_s = 2 kΩ, and C_p = 10 pF. Calculate the f_s and f_p of the crystal to three significant digits.

[Answers: 411 kHz, 412 kHz]

4.5 Relaxation (Nonsinusoidal) Oscillators:

The second major category of oscillators is the relaxation oscillator. Relaxation oscillators use an RC timing circuit and a device that changes states to generate a periodic waveform. In this section, we will learn about several circuits that are used to produce a waveform that is generally a square wave or other nonsinusoidal (triangular) waveform. Typically, a relaxation oscillator uses a Schmitt trigger or other device that changes states to alternately charge and discharge a capacitor through a resistor.

4.5.1 Hysteresis and Schmitt Trigger Oscillators:

Hysteresis is a property that means a device behaves differently when its input is increasing from the way it behaves when its input is decreasing. In the context of a voltage comparator, hysteresis means that the output will switch when the input increases to one level but will not switch back until the input falls below a different level. In some applications, hysteresis is a desirable characteristic because it prevents the comparator from switching back and forth in response to random noise fluctuations in the input.

Fig. 4-22(a) shows how hysteresis can be introduced into comparator operation. In this case, the input is connected to the inverting terminal and a voltage divider is connected across the noninverting terminal between v_o and a fixed reference voltage V_{REF} (which may be 0). Fig 4-22(b) shows the resulting ***transfer characteristic*** (called a ***hysteresis loop***). This characteristic shows that the output switches to $+V_{max}$ when v_{in} falls below a lower rigger level (LTL), but will not switch to $-V_{max}$ unless v_{in}, rises past an upper trigger level (UTL). The arrows indicate the portions of the characteristic followed when the input is increasing (upper line) and when it is decreasing (lower line). A comparator having this characteristic is called a ***Schmitt trigger***.

We can derive expressions for UTL and LTL using the superposition principle. Suppose first that the comparator output is shorted to ground. Then

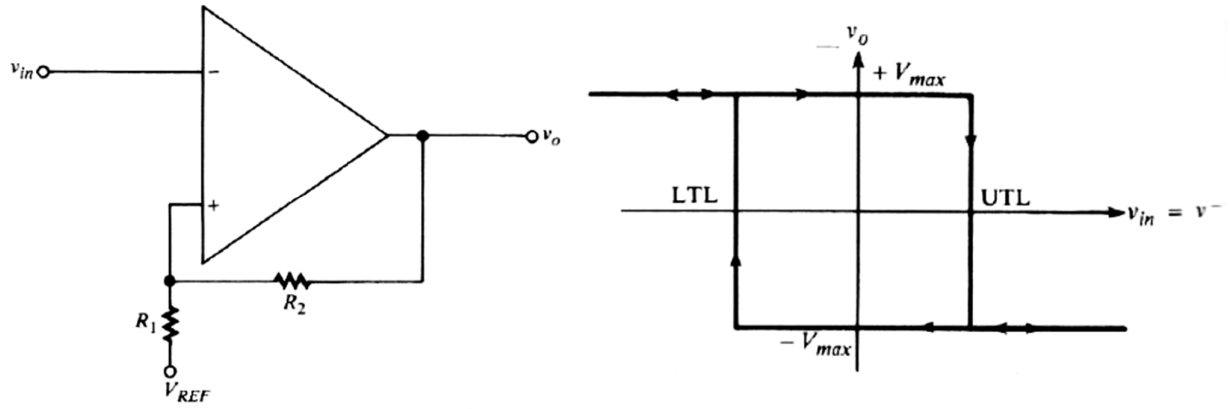
$$v^+ = \frac{R_2}{R_1+R_2}V_{REF} \quad (v_o = 0)$$

When V_{REF} is 0, we find

$$v^+ = \frac{R_1}{R_1+R_2}v_o \quad (V_{REF} = 0)$$

Therefore, when the output is at its negative limit ($v_o = -V_{max}$),

$$v^+ = \frac{R_2}{R_1+R_2}V_{REF} + \frac{R_1}{R_1+R_2}(-V_{max})$$



(a) (b)

Fig. 4-22

As can be seen in Fig. 4-22(b), v^- must ***fall***, to this value of v^+ before the comparator switches to $+V_{max}$. Therefore,

$$\text{LTL} = \frac{R_2}{R_1+R_2}V_{REF} + \frac{R_1}{R_1+R_2}(-V_{max}) \qquad [4\text{-}14]$$

Similarly, when $v_o = +V_{max}$, v_{in} must ***rise*** to

$$\text{UTL} = \frac{R_2}{R_1+R_2}V_{REF} + \frac{R_1}{R_1+R_2}(+V_{max}) \qquad [4\text{-}15]$$

In these equations, $+V_{max}$ is the maximum positive output voltage (a positive number) and $-V_{max}$ is the maximum negative output voltage (a negative number). The magnitudes of these quantities may be different; for example, $+V_{max} = 10$ V and $-V_{max} = -5$ V.

Quantitatively, the hysteresis of a Schmitt trigger is defined to be the difference between the input trigger levels. From Eqn. 4-14 and Eqn. 4-15,

$$\text{Hysteresis} = \text{UTL} - \text{LTL} = \frac{R_1}{R_1+R_2}(+V_{max}) - \frac{R_1}{R_1+R_2}(-V_{max}) \qquad [4\text{-}16]$$

If the magnitudes of the maximum output voltages are equal, we have

$$\text{Hysteresis} = \frac{2R_1V_{max}}{R_1+R_2} \qquad [4\text{-}17]$$

Exercise 4-5:

(a) Find the upper and lower trigger levels and the hysteresis of the Schmitt trigger shown in Fig. 4-23. Sketch the hysteresis loop. The output switches between ±15 V.

(b) Repeat (a) if $V_{REF} = 0$ V.

(c) Repeat (a) if $V_{REF} = 0$ V and the output switches between 0 V and +15 V.

[Answers: (a) −1V, +9V, 10V, (b) −5V, +5V, 10V, (c) 0V, +5V, 5V, Fig. 4-24]

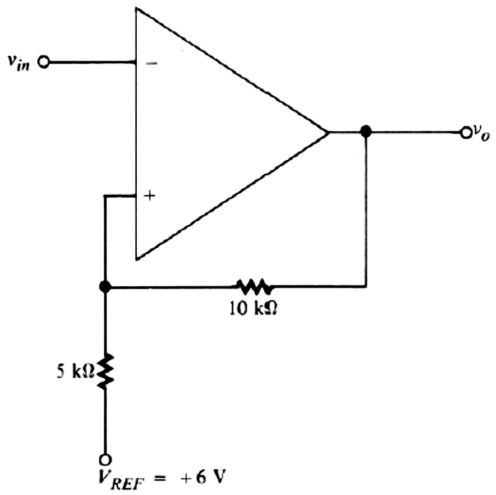


Fig. 4-23

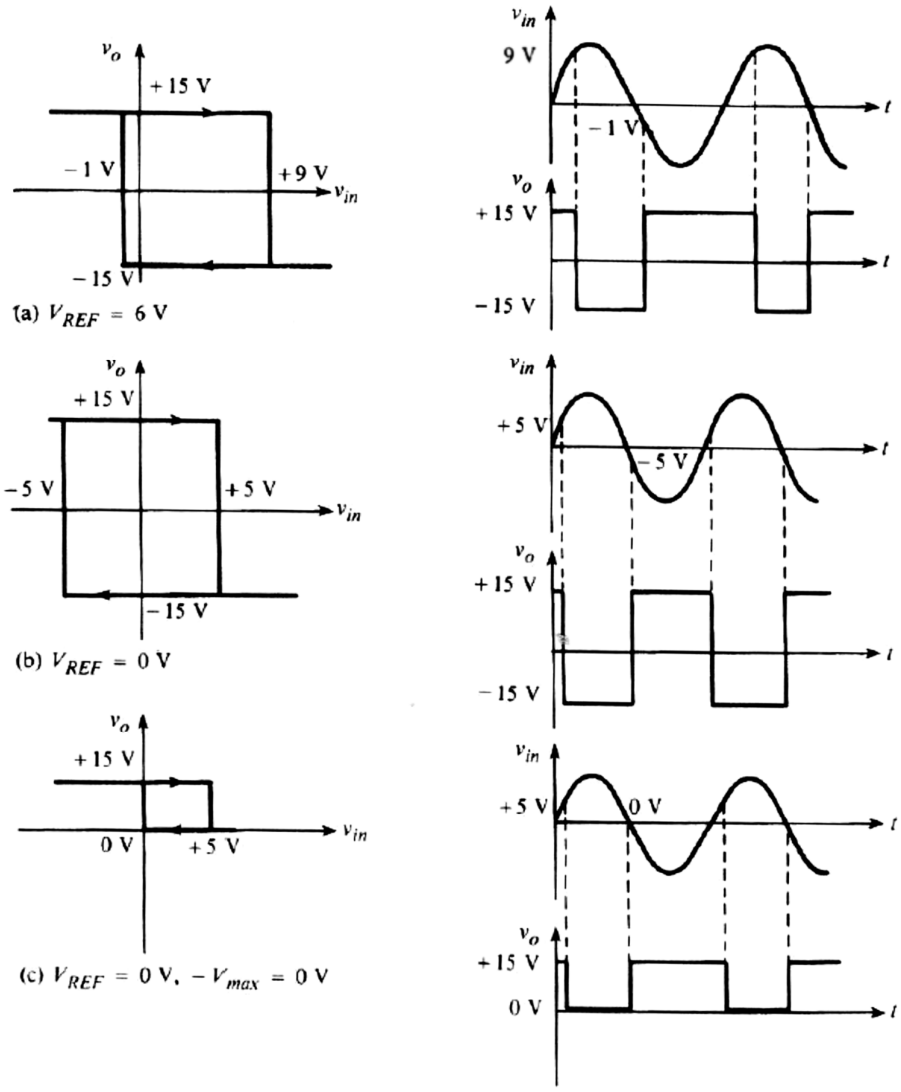
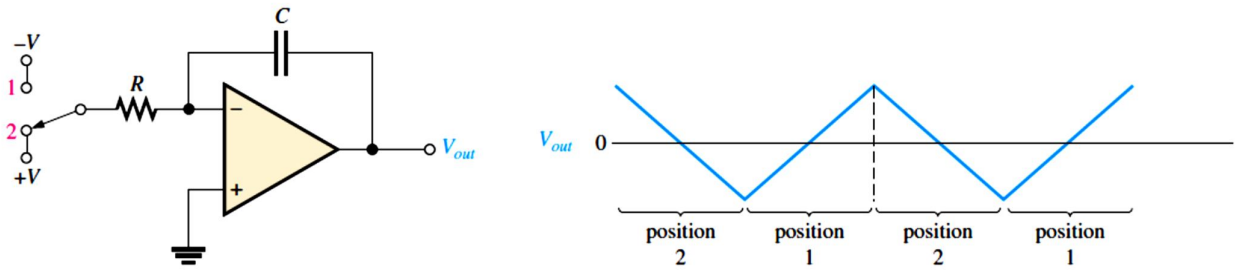


Fig. 4-24

4.5.2 A Triangular-Wave Oscillator:

The op-amp integrator can be used as the basis for a triangular-wave oscillator. The basic idea is illustrated in Fig. 4-25(a) where a dual-polarity, switched input is used. We use the switch only to introduce the concept; it is not a practical way to implement this circuit. When the switch is in position 1, the negative voltage is applied, and the output is a positive-going ramp. When the switch is thrown into position 2, a negative-going ramp is produced. If the switch is thrown back and forth at fixed intervals, the output is a triangular wave consisting of alternating positive-going and negative-going ramps, as shown in Fig. 4-25(b).



(a) (b)

Fig. 4-25

One practical implementation of a triangular wave oscillator utilizes an op-amp comparator with hysteresis to perform the switching function, as shown in Fig. 4-26. The operation is as follows. To begin, assume that the output voltage of the comparator is at its maximum negative level. This output is connected to the inverting input of the integrator through R_1, producing a positive-going ramp on the output of the integrator. When the ramp voltage reaches the upper trigger point (UTP), the comparator switches to its maximum positive level. This positive level causes the integrator ramp to change to a negative-going direction. The ramp continues in this direction until the lower trigger point (LTP) of the comparator is reached. At this point, the comparator output switches back to the maximum negative level and the cycle repeats. This action is illustrated in Fig. 4-27.

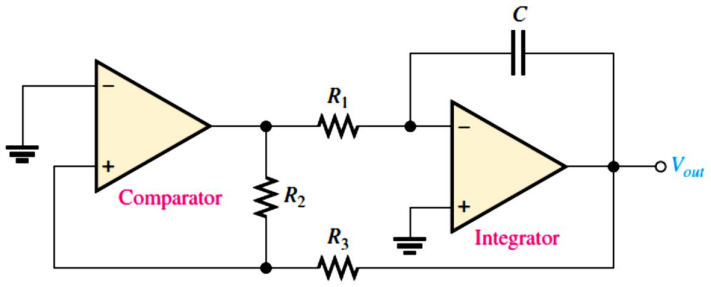


Fig. 4-26

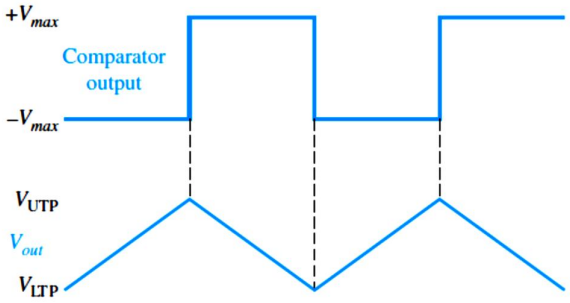


Fig. 4-27

Since the comparator produces a square-wave output, the circuit in Fig. 4-26 can be used as both a triangular-wave oscillator and a square-wave oscillator. Devices of this type are commonly known as ***function generators*** because they produce more than one output function. The output amplitude of the square wave is set by the output swing of the comparator, and the resistors R_2 and R_3 set the amplitude of the triangular output by establishing the UTP and LTP voltages according to the following formulas:

$$V_{\text{UTP}} = +V_{max}\left(\frac{R_3}{R_2}\right) \qquad [4\text{-}18]$$

$$V_{\text{LTP}} = -V_{max}\left(\frac{R_3}{R_2}\right) \qquad [4\text{-}19]$$

where the comparator output levels, $+V_{max}$ and $-V_{max}$ are equal. The frequency of both waveforms depends on the time constant as well as the amplitude-setting resistors, R_2 and R_3. By varying R_1, the frequency of oscillation can be adjusted without changing the output amplitude.

$$f_r = \frac{1}{4R_1C}\left(\frac{R_2}{R_3}\right) \qquad [4\text{-}20]$$

Exercise 4-6:

Determine the frequency of oscillation of the circuit in Fig. 4-28. To what value must R_1 be changed to make the frequency 20 kHz?

[Answers: 8.25 kHz, 4.13 kΩ]

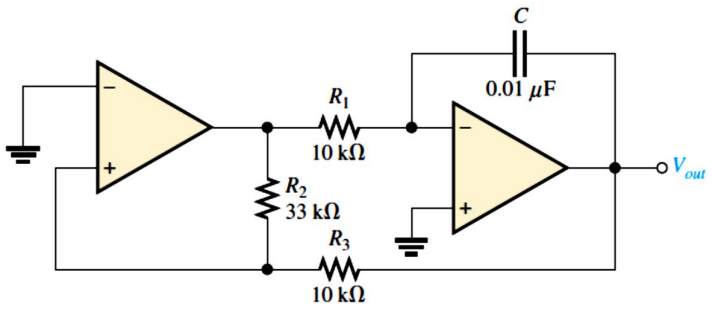


Fig. 4-28

4.5.3 A Square-Wave Oscillator (An Astable Multivibrator):

The word ***astable*** means "unstable" and, like other unstable devices, an astable multivibrator is a (***square-wave***) oscillator. (A ***bistable*** multivibrator, also called a ***flip-flop***, is a digital device with two stable states; a ***monostable*** multivibrator has one stable state, and an astable multivibrator has zero stable states.) An astable multivibrator can be constructed by using an operational amplifier as a voltage comparator in a circuit like that shown in Fig. 4-29.

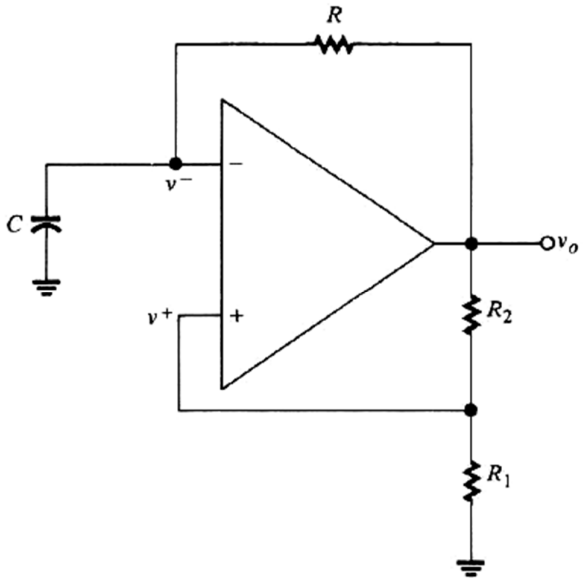


Fig. 4-29

For analysis purposes, let us assume that the output voltages of the comparator are equal in magnitude and opposite in polarity: $\pm V_{max}$. Fig. 4-30 shows the voltage across capacitor C and the output waveform produced by the comparator. We begin by assuming that the output is at $+V_{max}$. Then, the voltage fed back to the noninverting input is

$$v^+ = \frac{R_1}{R_1+R_2}(+V_{max}) = +\beta V_{max} \qquad [4\text{-}21]$$

Notice that v^- equals the voltage across the capacitor. The capacitor begins to charge through R towards a final voltage of $+V_{max}$. However, as soon as the capacitor voltage reaches a voltage equal to v^+, the comparator switches state. In other words, switching occurs at the point in time where $v^- = v^+ = +\beta V_{max}$. After the comparator switches state, its output is $-V_{max}$, and the voltage fed back to the noninverting input becomes

$$v^+ = \frac{R_1}{R_1+R_2}(-V_{max}) = -\beta V_{max} \qquad [4\text{-}22]$$

Since the comparator output is now negative, the capacitor begins to discharge through R towards $-V_{max}$. But, when that voltage falls to $-\beta V_{max}$, we once again have $v^+ = v^-$, and the comparator switches back to $+V_{max}$. This cycle repeats continuously, as shown in Fig. 4-30, with the result that the output is a square wave that alternates between $\pm V_{max}$ volts.

It can be shown that the period of the multivibrator oscillation is

$$T = 2RC \ln\left(\frac{1+\beta}{1-\beta}\right) \qquad [4\text{-}23]$$

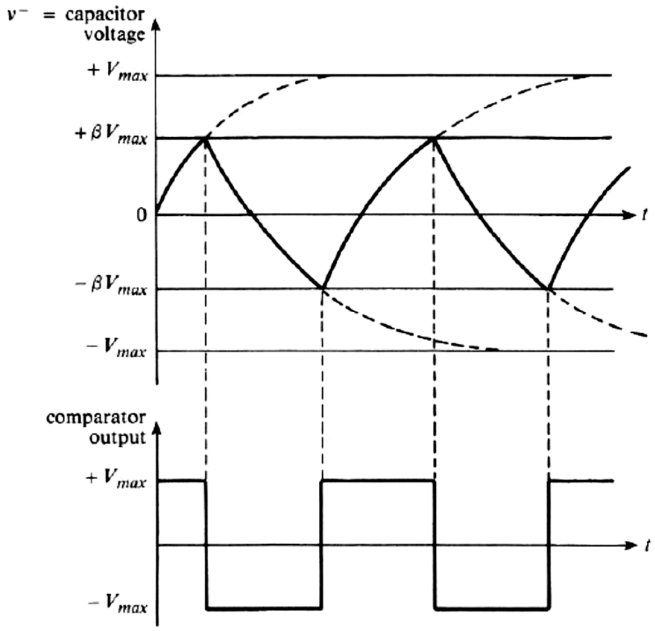


Fig. 4-30

4.5.4 The 555 Timer as an Oscillator:

The 555 timer consists basically of two comparators, a flip-flop, a discharge transistor, and a resistive voltage divider, as shown in Fig. 4-31. The flip-flop (bistable multivibrator) is a two-state device whose output can be at either a high voltage level (set, *S*) or a low voltage level (reset, *R*). The state of the output can be changed with proper input signals.

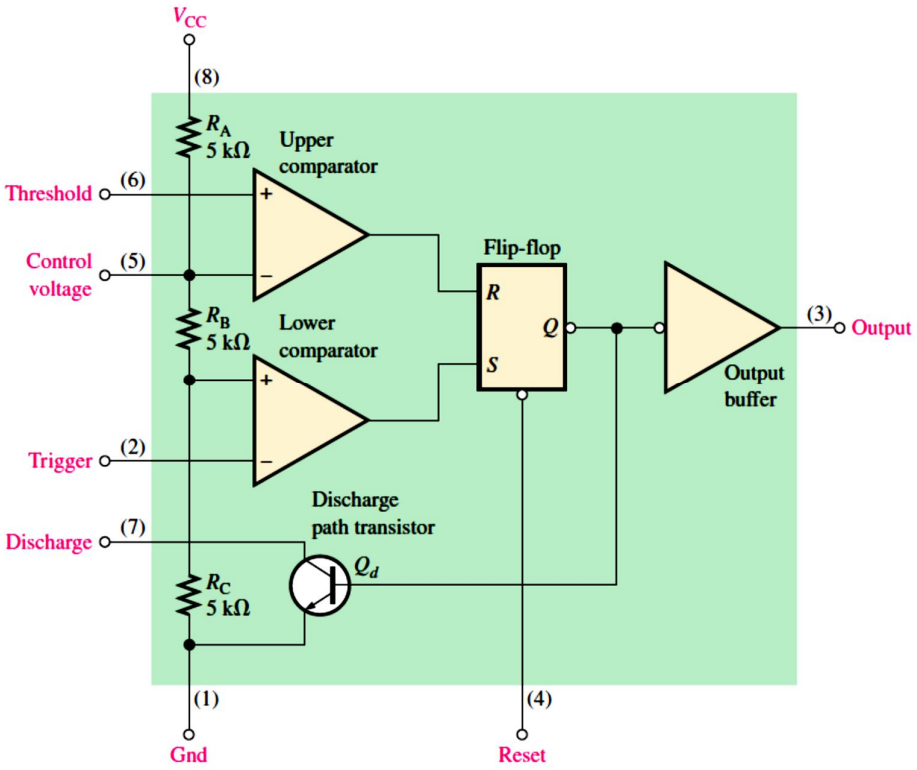


Fig. 4-31

The resistive voltage divider is used to set the voltage comparator levels. All three resistors are of equal value; therefore, the upper comparator has a reference of $^2/_3V_{CC}$, and the lower comparator has a reference of $^1/_3V_{CC}$. The comparators' outputs control the state of the flip-flop. When the trigger voltage goes below $^1/_3V_{CC}$, the flip-flop sets and the output jumps to its high level. The threshold input is normally connected to an external *RC* timing circuit. When the external capacitor voltage exceeds $^2/_3V_{CC}$, the upper comparator resets the flip-flop, which in turn switches the output back to its low level. When the device output is low, the discharge transistor (Q_d) is turned on and provides a path for rapid discharge of the external timing capacitor. This basic operation allows the timer to be configured with external components as an oscillator, a one-shot, or a time delay element.

A 555 timer connected to operate in the astable mode as a free-running relaxation oscillator (astable multivibrator) is shown in Fig. 4-32. The threshold input (THRESH) is now connected to the trigger input (TRIG). The external components R_1, R_2, and C_{ext} form the timing circuit that sets the frequency of oscillation. The 0.01 µF capacitor connected to the control (CONT) input is strictly for decoupling and has no effect on the operation.

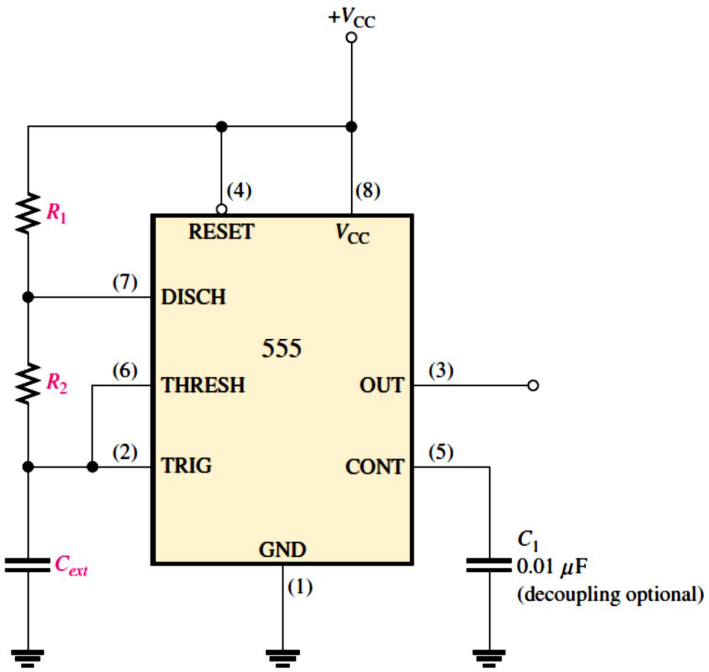


Fig. 4-32

Initially, when the power is turned on, the capacitor C_{ext}, is uncharged and thus the trigger voltage (pin 2) is at 0 V. This causes the output of the lower comparator to be high and the output of the upper comparator to be low, forcing the output of the flip-flop, and thus the base of Q_d, low and keeping the transistor off. Now, C_{ext} begins charging through $R1$ and R_2 as indicated in Fig. 4-33. When the capacitor voltage reaches $^1/_3V_{CC}$, the lower comparator switches to its low output state, and when the capacitor voltage reaches $^2/_3V_{CC}$, the upper comparator switches to its high output state. This resets the flip-flop, causes the base of Q_d to go high, and turns on the transistor. This sequence creates a discharge path

for the capacitor through R_2 and the transistor, as indicated. The capacitor now begins to discharge, causing the upper comparator to go low. At the point where the capacitor discharges down to $\frac{1}{3}V_{CC}$, the lower comparator switches high, setting the flip-flop, which makes the base of Q_d low and turns off the transistor. Another charging cycle begins, and the entire process repeats. The result is a rectangular wave output whose duty cycle depends on the values of R_1 and R_2. The frequency of oscillation is given by Eqn. 4-24, or it can be found using the graph in Fig. 4-34.

$$f_r = \frac{1.44}{(R_1+2R_2)C_{ext}} \qquad [4\text{-}24]$$

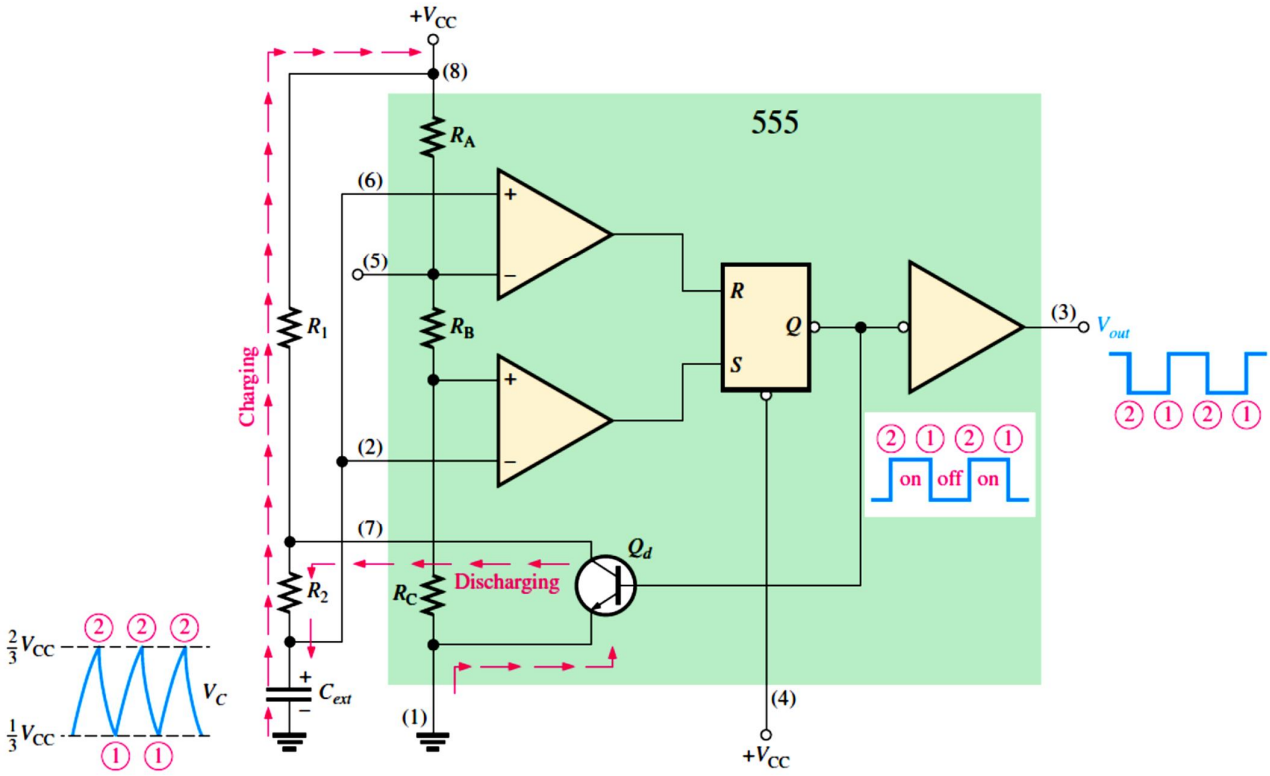


Fig. 4-33

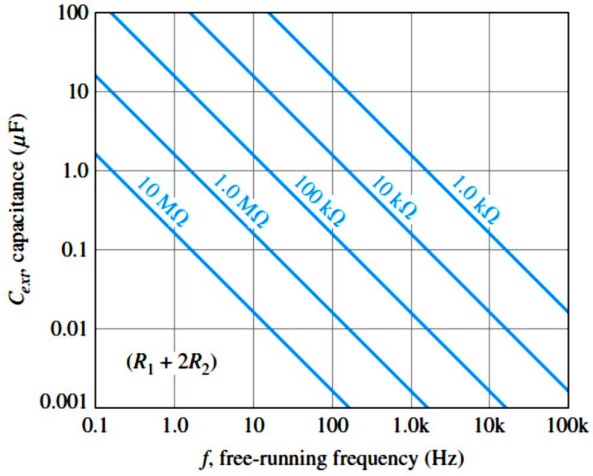


Fig. 4-34

By selecting R_1 and R_2, the duty cycle of the output can be adjusted. Since C_{ext} charges through $R_1 + R_2$ and discharges only through R_2, duty cycles approaching a minimum of 50 percent can be achieved if $R_2 >> R_1$ so that the charging and discharging times are approximately equal.

A formula to calculate the duty cycle is developed as follows. The time that the output is high (t_H) is how long it takes C_{ext} to charge from $\frac{1}{3}V_{CC}$ to $\frac{2}{3}V_{CC}$. It is expressed as

$$t_H = 0.694(R_1 + R_2)C_{ext} \quad [4\text{-}25]$$

The time that the output is low (t_L) is how long it takes to discharge from $\frac{2}{3}V_{CC}$ to $\frac{1}{3}V_{CC}$. It is expressed as

$$t_L = 0.694R_2C_{ext} \quad [4\text{-}26]$$

The period, T, of the output waveform is the sum of t_H and t_L. The following formula for T is the reciprocal of f_r in Eqn. 4-24.

$$T = \frac{1}{f_r} = t_H + t_L = 0.694(R_1 + 2R_2)C_{ext} \quad [4\text{-}27]$$

Finally, the percent duty cycle is

$$\text{Duty cycle} = \left(\frac{t_H}{T}\right)100\% = \left(\frac{t_H}{t_H + t_L}\right)100\% = \left(\frac{R_1 + R_2}{R_1 + 2R_2}\right)100\% \quad [4\text{-}28]$$

To achieve duty cycles of less than 50 percent, the circuit in Fig 4-32 can be modified so that C_{ext} charges through only R_1 and discharges through R_2. This is achieved with a diode, D_1, placed as shown in Fig. 4-35. The duty cycle can be made less than 50 percent by making R_1 less than R_2. Under this condition, the formulas for the frequency and percent duty cycle are (assuming an ideal diode)

$$f_r \cong \frac{1.44}{(R_1 + R_2)C_{ext}} \quad [4\text{-}29]$$

$$\text{Duty cycle} \cong \left(\frac{R_1}{R_1 + R_2}\right)100\% \quad [4\text{-}30]$$

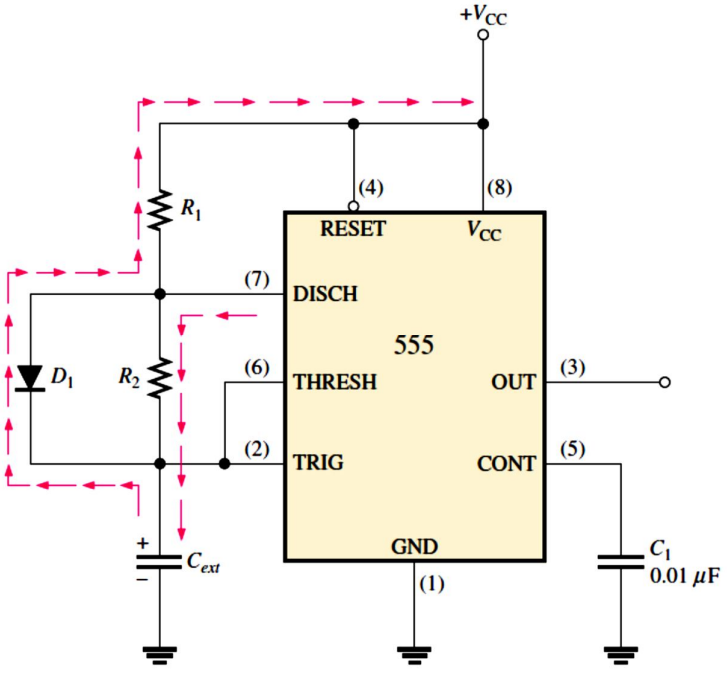


Fig. 4-35

A 555 timer can be set up to operate as a voltage-controlled oscillator (VCO) by using the same external connections as for astable operation, with the exception that a variable control voltage is applied to the CONT input (pin 5), as indicated in Fig. 4-36.

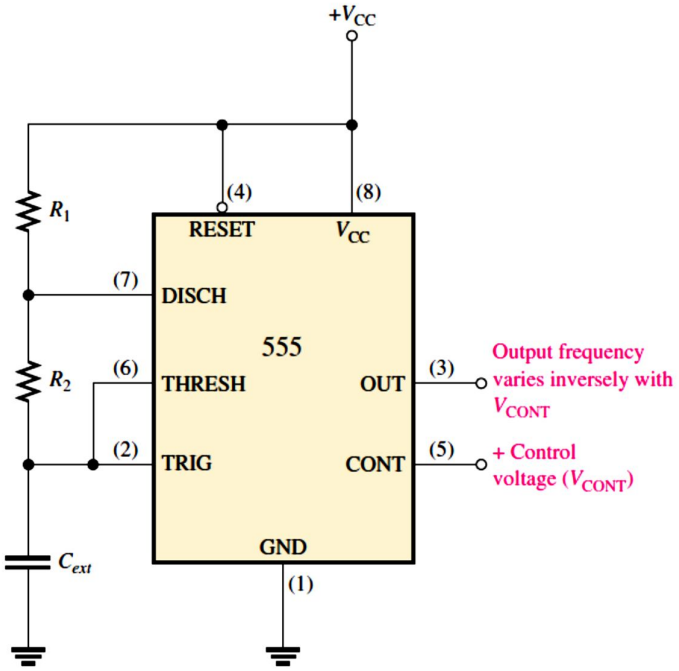


Fig. 4-36

As shown in Fig. 4-37, the control voltage (V_{CONT}) changes the threshold values of $\frac{1}{3}V_{CC}$ and $\frac{2}{3}V_{CC}$ for the internal comparators. With the control voltage, the upper value is V_{CONT} and the lower value is $\frac{1}{2}V_{CONT}$, as we can see by examining the internal diagram of the 555 timer. When the control voltage is varied, the output frequency also varies. An increase in V_{CONT} increases the charging and discharging time of the external capacitor and causes the frequency to decrease. A decrease in decreases the charging and discharging time of the capacitor and causes the frequency to increase.

An interesting application of the VCO is in phase-locked loops, which are used in various types of communication receivers to track variations in the frequency of incoming signals.

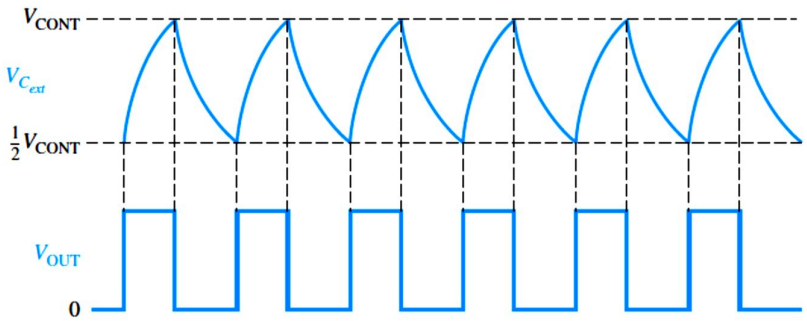


Fig. 4-37

Exercise 4-7:

A 555 timer configured to run in the astable mode (oscillator) is shown in Fig. 4-38. Determine the frequency of the output and the duty cycle.

[Answers: 5.64 kHz, 59.5%]

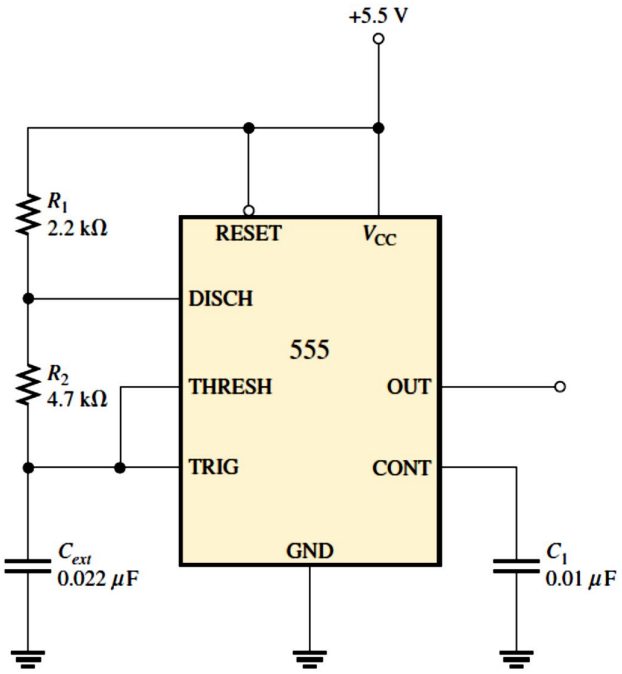


Fig. 4-38

MODULE 6

CS 205

ZENER DIODE AS A VOLTAGE REGULATOR

Zener diode :

In the reverse bias pn-junction, it has been noted that when the reverse voltage applied to the pn-junction increases, at a critical voltage called as breakdown voltage the reverse current increases sharply to a high value. The breakdown region is the knee of the reverse characteristics as shown in figure.

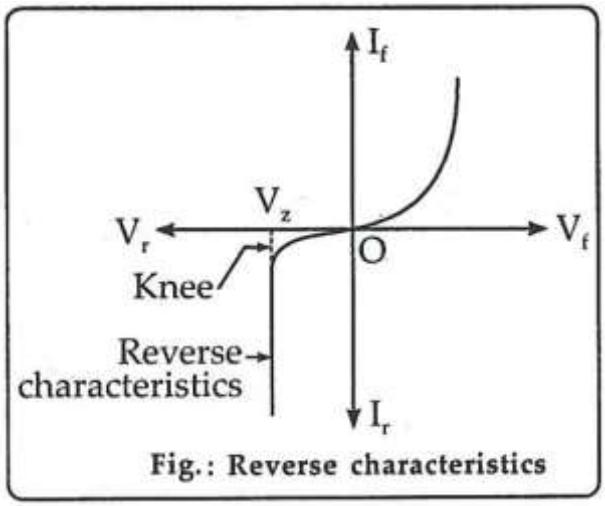


Fig.: Reverse characteristics

The satisfactory explanation of this breakdown of the junction was first given by the American scientist C. Zener. Therefore, breakdown voltage is sometimes called the Zener voltage and the sudden increase in current is called Zener current. The breakdown or Zener voltage depends upon the amount of doping. If the diode is heavily doped, depletion layer will be thin and consequently the breakdown of the junction will occur at a lower reverse voltage. On the other hand, a lightly doped diode has a higher breakdown voltage. When an ordinary pn-junction diode is properly doped so that it has a sharp breakdown voltage is called as Zener diode.

Definition: *"A properly doped pn-jinction diode which has a sharp breakdown voltage is called a Zener diode."*
The symbol of Zener diode is as shown in following figure.

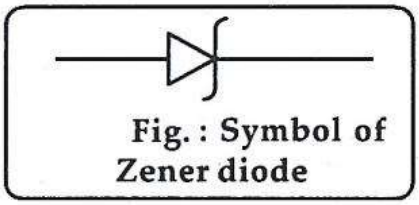


Fig. : Symbol of Zener diode

It should be noted that, it is just like an ordinary diode except that the bar is turned into Z-shape. The following points should be noted about the **Zener diode**

1. A Zener diode is always reverse connected, i.e. it is reverse biased.

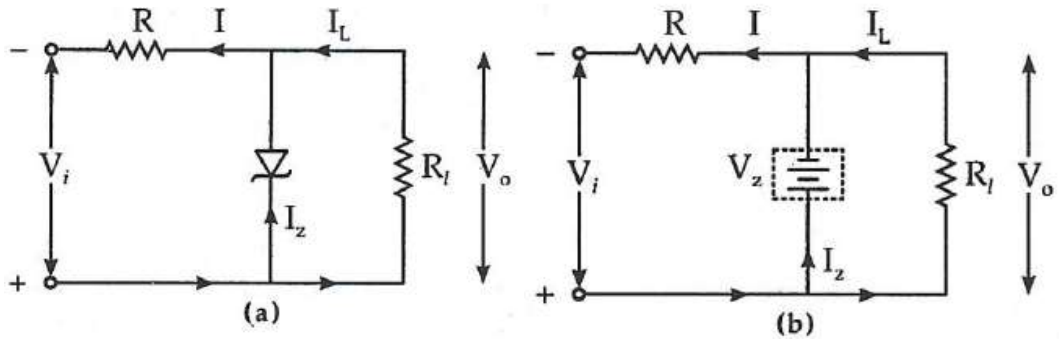
2. A Zener diode has sharp breakdown voltage, called Zener voltage (Vz).
3. When forward biased, its characteristics are just those of an ordinary diode.
   A large current flows through zener diode at breakdown because of two effects called as zener effect and avalanche effect.

Zener effect : When applied reverse voltage is breakdown voltage or more, large number of electron hole pairs are generated because they are pulled from covalent bonds therefore current suddenly increases this is called as zener effect.

Avalanche effect: At breakdown voltage minority current carriers are accelerated in the depletion layer. When they are accelerate, collision with other atoms takes place. This generates new electrons which are again accelerated so more atoms gets ionized and thus a bunch of electrons or a avalanche of electrons is produced which increases the reverse current through zener. This is called as avalanche effect.

Zener diode as a voltage regulator :

A Zener diode can be used as a voltage regulator to provide a constant voltage from a source whose voltage may vary over sufficient range. The circuit diagram of use of Zener diode as a voltage regular is as shown in following figure.(a) The Zener diode of Zener voltage Vz is reverese Connected across the load R_l across which constant output is desired. The series resistance R absorbs the output voltage fluctuations so as tq maintain constant voltage across the load. It may be noted that the Zener will maintain constant Vz (= V0) across the load so long as the input voltage does not fall below Vz. When the circuit is properly designed, the load voltage V0 remains constant (equal to Vz) even though the input voltage Vi and load resistance may vary over a wide range.



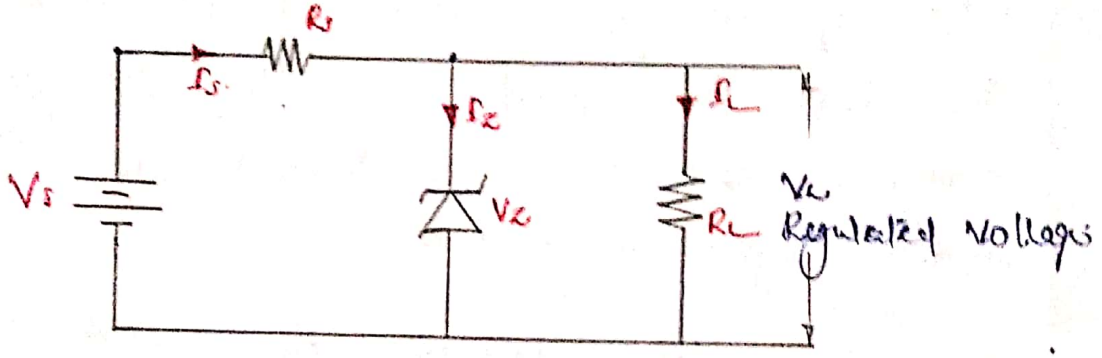
Suppose the input voltage increases. Since the Zener is in the breakdown region, the Zener diode is equivalent to a battery Vz as shown in figure (b).

It is clear that output voltage remains constant at Vz (= V0). The excess voltage is dropped across the series resistance R. This will cause an increase in the .value of total current I. The Zener will conduct the increase of current in I while the load current remains constant. Hence, output voltage V_0 remains constant irrespective of the change in the input voltage Vi.
Now suppose that the input voltage is constant but the load resistance decreases, this will cause an increase in load current. The extra current cannot come from the source because drop in R (and hence source current I) will not change as the Zener is within its regulating range. The additional load current 'will come from a decrease in Zener current Iz. Consequently, the output voltage stays at constant value. Voltage drop across R = Vi - V0 and current through R is $I = Iz + I_L$

MODULE 5
REGULATED POWER SUPPLIES:

Zener Voltage Regulator: (12)

Zener diode voltage regulator is a shunt regulator because zener is connected in parallel with load. The resistance R_s is used to limit current in the ckt. Regulated op voltage is obtained across load R_L



$V_s = I_s R_s + V_z$ ---(1); $I_s = \frac{V_s - V_z}{R_s}$ ---(2)

load voltage $V_L = V_z$.

$I_s = I_z + I_L$ ---(3)

$I_z = I_s - I_L$

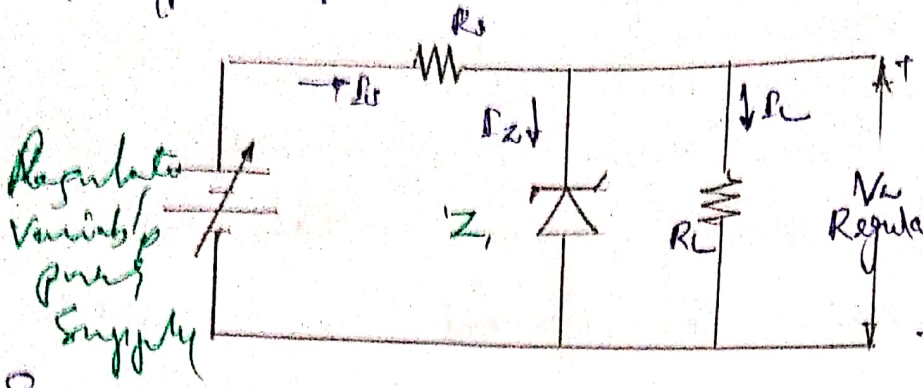
From eqn (2) $\Rightarrow$ $R_s = \frac{V_s - V_o}{I_z + I_L}$

$R_{s\,max} = \frac{V_{s\,max} - V_o}{I_{L\,min} + I_{z\,max}}$

$R_{s\,min} = \frac{V_{s\,max} - V_o}{I_{L\,max} + I_{z\,min}}$

* Line Regulation

In this case load resistance R_L is kept constant and i/p voltage V_s is varied.



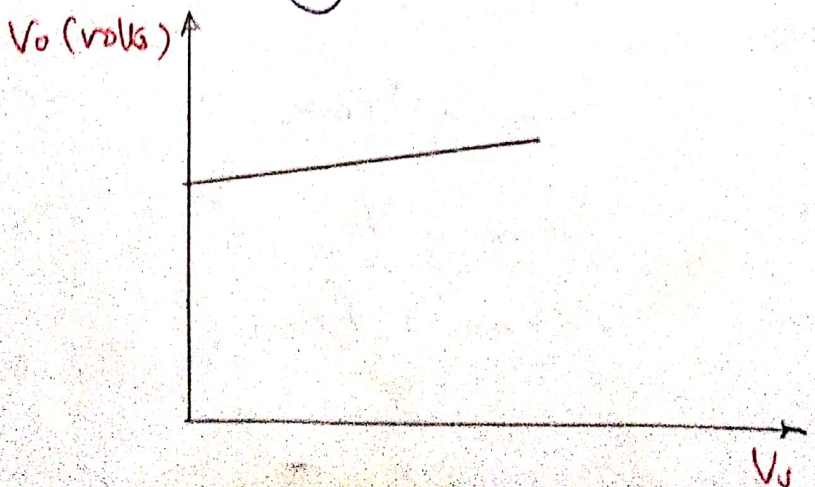
Since $I_s = I_z + I_L$

when o/p voltage increases I_s also increases. This increased current will flow through the zener with out affecting load current I_L. Hence keeping load voltage V_L constant.

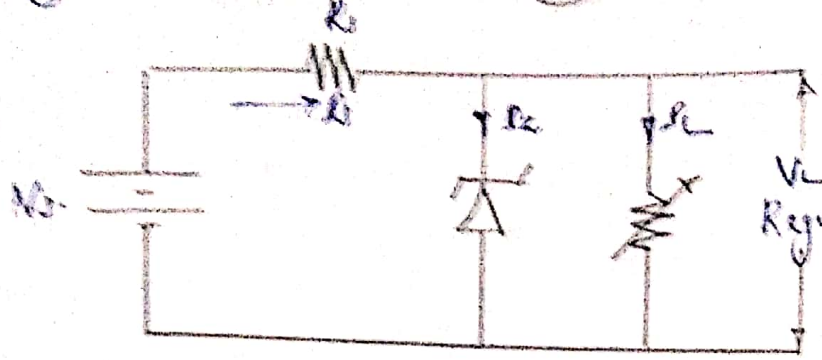
when i/p voltage decreases i/p current also decreases. Due to this current through zener decreases & also the voltage drop across series resistor decreases. Hence load voltage & load current remain constant.

- Line regulation Graph is plotted between i/p voltage & o/p voltage

Percentage regulation = $\frac{\Delta V_o}{\Delta V_s} \times 100$.



* Load Regulation



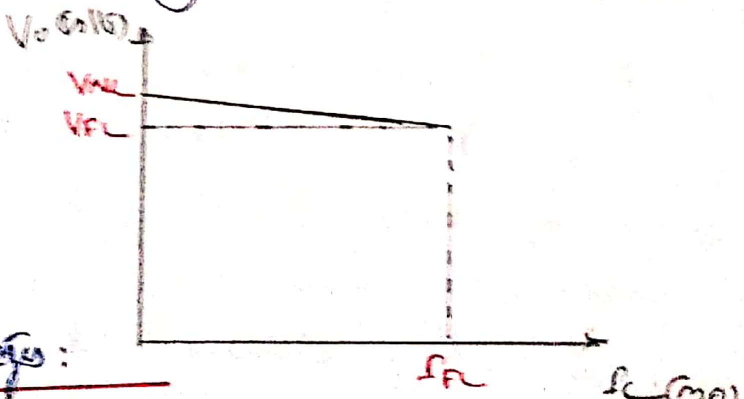
When V_s is kept fixed & R_L is varied.

When R_L decreases load current increases. This causes I_z to decreases. I_s & voltage across R_s remains const. $\therefore$ V_L is const.

When R_L increases load current decreases. Due to this zener current increases. This again keeps the values of i/p current & voltage drop across R_s as const $\therefore$ o/p voltage remain const.

Load regulation graph is plotted with load current on x axis & o/p voltage on y axis.

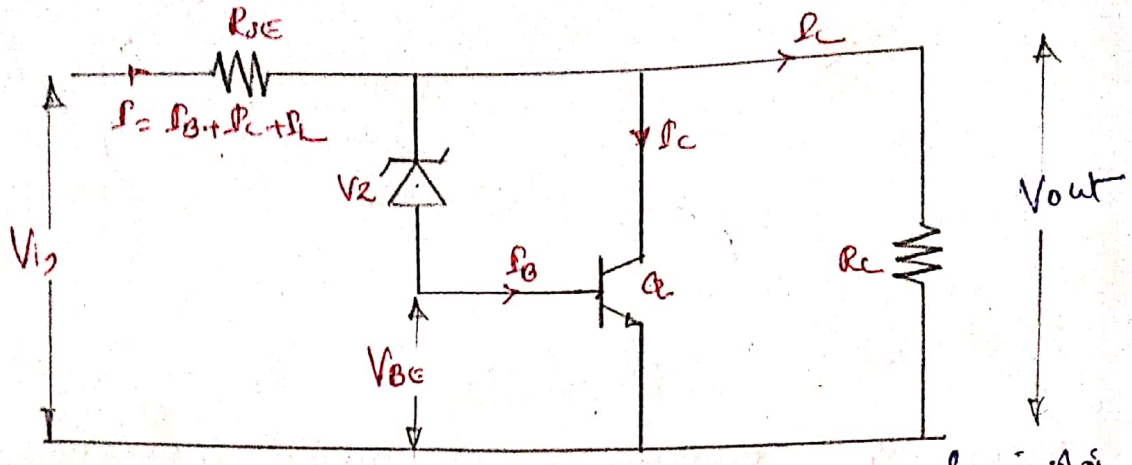
$$\text{Percentage regulation} = \frac{V_{NL} - V_{FL}}{V_{NL}} \times 100$$



Disadvantages:

* It is a fixed voltage regulator & cannot be made adjustable.
* Large power gets dissipated in series resistor R_s.
* Corresponding to large changes in load current there will be large changes in zener current. This results in large power wastage.

: Shunt Voltage Regulator Using Transistors:



A shunt voltage regulator using npn transistor & zener diode is shown. R_{SE} is connected in series with input voltage source and the voltage across load is fixed by zener diode and transistor base-emitter voltage V_{BE}

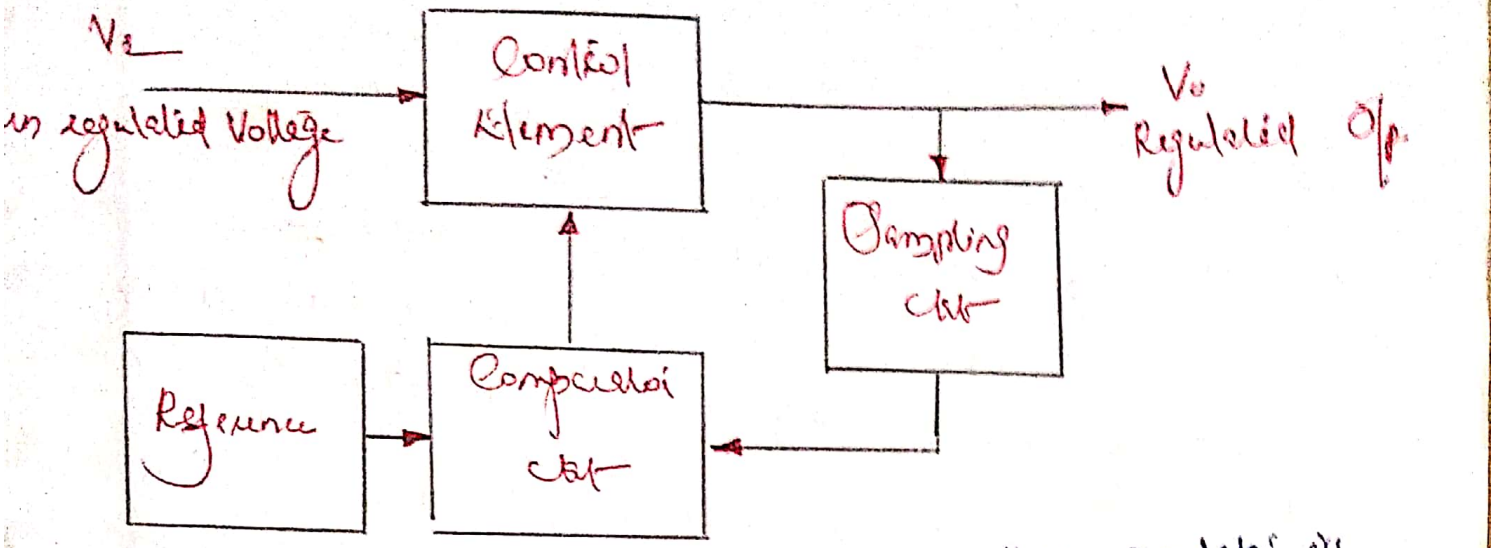
$$V_o = V_Z + V_{BE} = V_{in} - I.R_{SE}$$

Since both V_Z & V_{BE} remain nearly constant V_{out} remains constant.

If input voltage increases I will increase and increased base current I_B results in increased collector current I_C keeping I_L constant and there by V_{out} const. Reverse happens when supply voltage decreases

when R_L decreases I_L increases and this increased I_L is supplied by decrease in I_B and collector current I_C. $\therefore$ I remains const. $\therefore$ V_R is constant and $\therefore$ Vout is also constant Since V_S is constant. Reverse happens when load R_L increases.

Series Voltage Regulator:



The basic connection of Series voltage regulator is shown. The series element controls the amount of input voltage that gets to o/p. The o/p voltage is sampled by a ckt that provides feedback voltage to be compared to reference voltage.

* If o/p voltage increases, the comparator ckt provides a control signal to cause series control element to decrease the amount of o/p voltage, thus by maintaining o/p voltage.
* If the o/p voltage decreases, the comparator ckt provides a control signal to cause series control element to increase the amount of o/p voltage.

Emitter follower Series pass Regulator:

The power transistor used in this configuration is known as pass transistor. Because of the current amplifying property of transistor

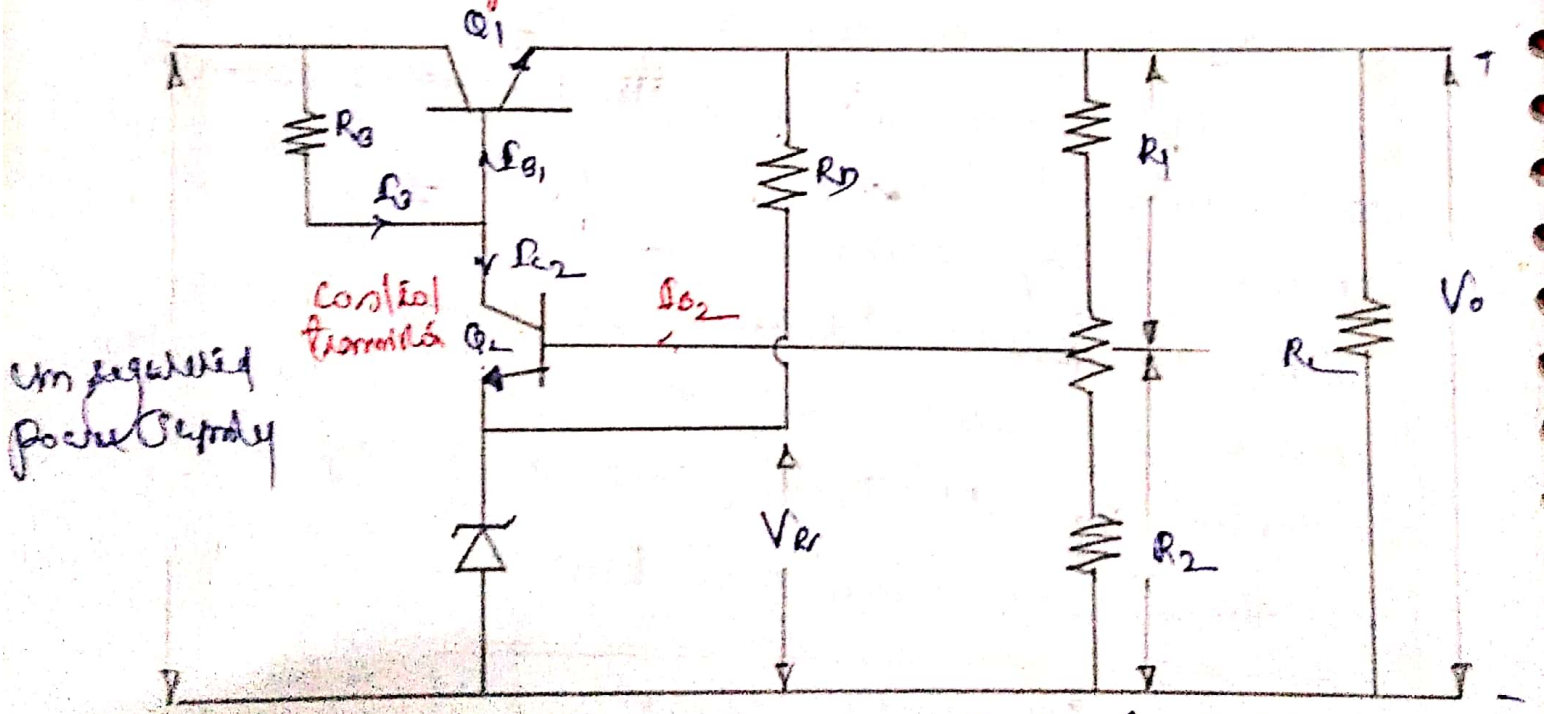
the current in zener diode is small. Hence there is little drop across diode and zener approximates an ideal constant voltage source

Transistor Q_1 is the series control element and zener diode provides reference voltage. The regulating operation is as follows.

* If o/p voltage decreases, increased base emitter voltage causes transistor Q_1 to conduct more there by raising o/p voltage - maintaining o/p constant
* If the o/p voltage increases, the decreased base emitter voltage causes Q_1 to conduct less there by reducing o/p voltage. - maintaining o/p constant.

Series pass transistor Voltage Regulator.

Series pass transistor



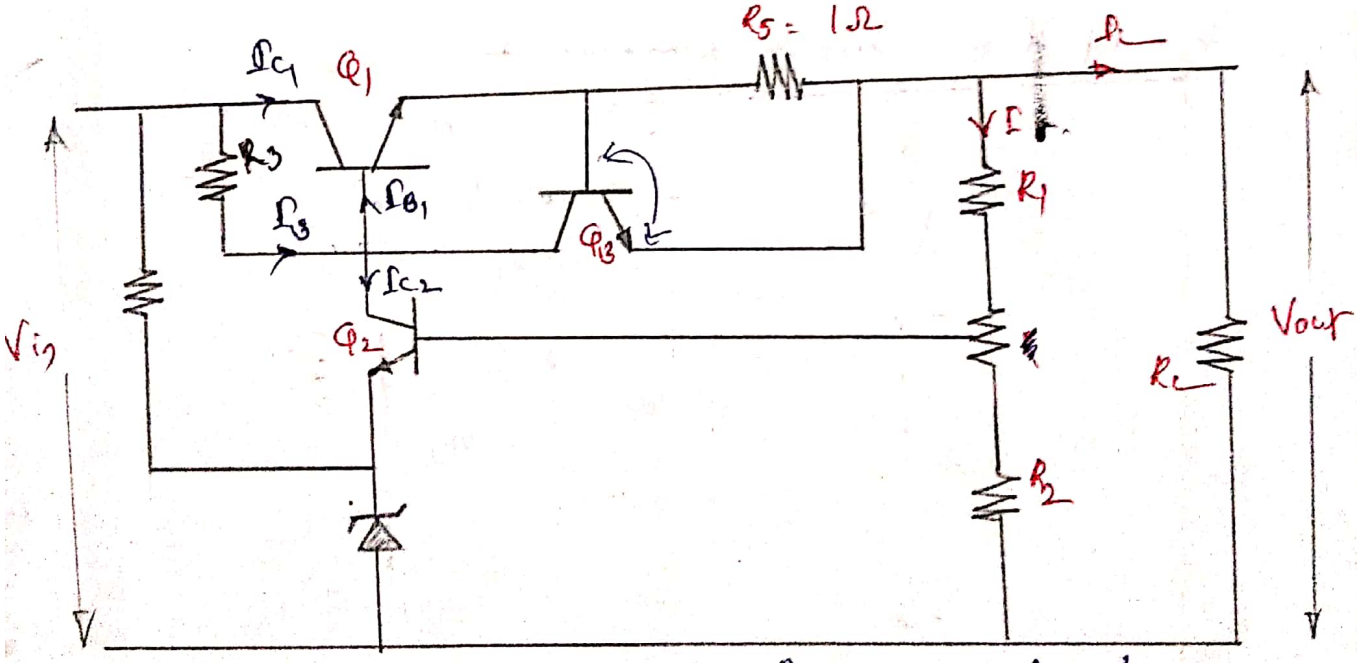
Here the control voltage transistor Q_2's emitter terminal is connected to -ve terminal of supply through zener diode

The voltage regulator employs the principle of negative feedback to hold o/p voltage almost constant.

Q_1 is the pass transistor because all load current flows through it.

If the o/p voltage increases, the voltage across R_2 is also increases. This causes increase in base bias of Q_2; as a result I_{B_2} and I_{C_2} increases. Assuming I_B constant, I_{B_1} decreases. Decrease in base current of transistor Q_1 causes increase in collector-emitter resistance of Q_1. This causes increase in V_{CE_1} and offsetting the increase in o/p voltage. Thus o/p voltage remains constant. Reverse happens when the o/p voltage decreases.

* Controlled transistor Series Regulator with Overload & Short Circuit protection. *



If the load resistance R_L is reduced or load terminals are shorted accidently, a very large current will flow in the ckt; it may destroy the pass transistor Q_1.

- To avoid this situation current limiting ckt is added to series regulator.

The current limiting ckt consists of transistor Q_3 and resistor R_5 connected b/w base and emitter of Q_3.

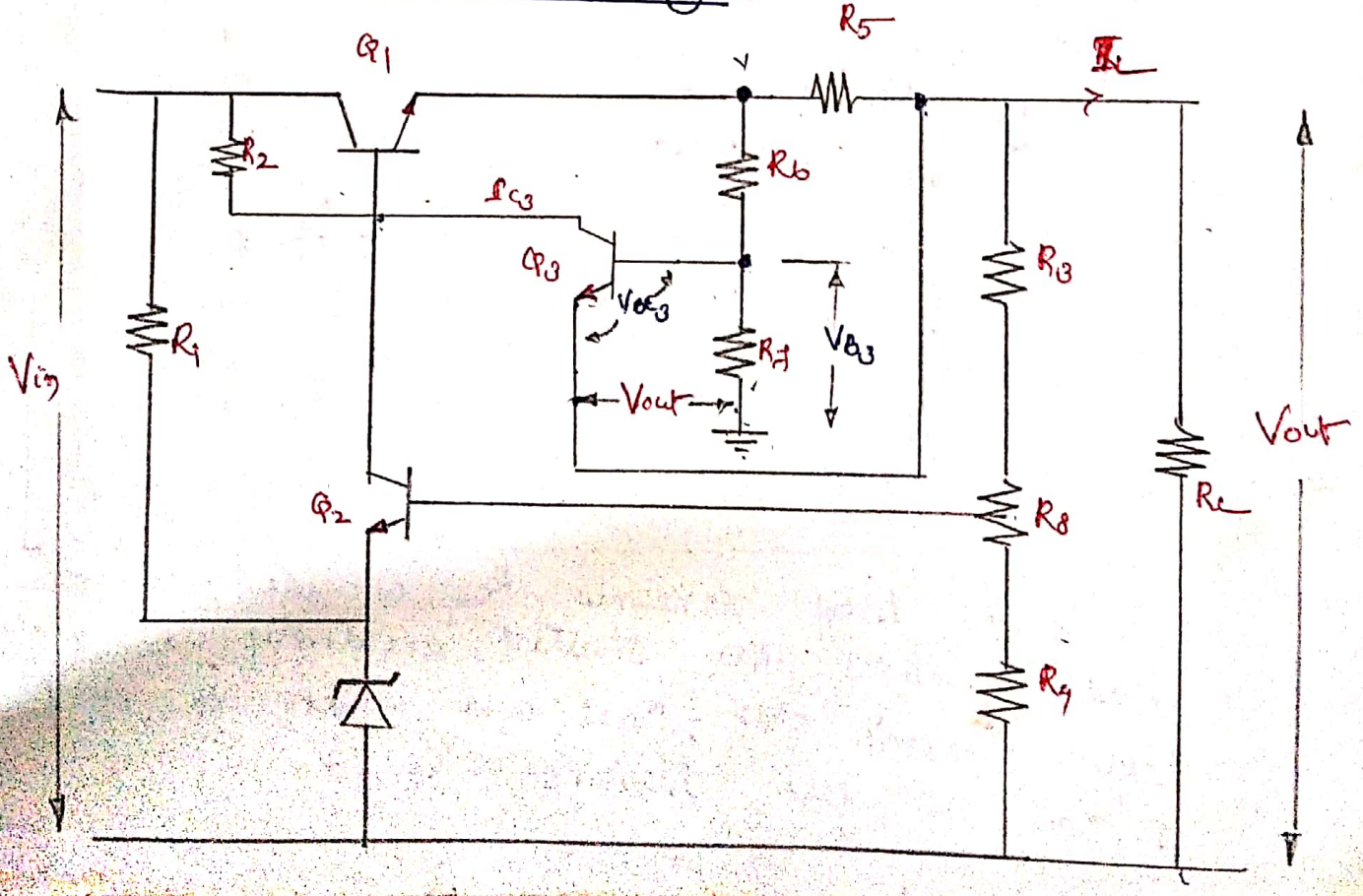
With normal load current, Q_3 remains off because the voltage drop across R_5 is small. Under this condition ckt works normally.

With excessive load current [exceeding $\frac{0.6}{1} = 0.$ or 600mA] the voltage drop across R_5 is enough to turn ON transistor Q_3. The collector current of Q_3 flows through R_3 decreasing base voltage of Q_1. This results in reduction of conduction level of Q_1. Thus further increase in load current is prevented.

Power dissipation across pass transistor

$$P_V = (V_{in} - V_{BE}) I_{SC}$$

* Fold back Current limiting: *



In short circuit protection Rsc is large amount of power dissipating in circuit then transistor Q_1 enter the regulation region from saturation.

In foldback circuit base of Q_3 is biased by voltage divider n/w of R_5 & R_4 the load current I_L flows through R_5 causing drop across it. Thus voltage of $(I_L R_5 + V_{out})$ acts across (R_4 & R_4) n/w. The voltage applied to base of Q_3 is equal to the voltage drop across R_4 and is

$$V_{B3} = \frac{R_4}{R_5 + R_4}\left[I_L R_5 + V_{out}\right] = k\left[I_L R_5 + V_{out}\right]$$

$$V_{BE3} = V_{B3} - V_{out} = k\left[I_L R_5 + V_{out}\right] - V_{out}$$

$$V_{BE3} = k I_L R_5 + (k-1)V_{out}$$

Now if load resistance decrease, load current I_L will increase causing drop $I_L R_5$ to increase. This makes V_{B3} to increase & $\therefore$ V_{BE3} will also increase and Q_3 will conduct more. The increased collector current I_{C3} of transistor Q_3 flows through R_3 decreasing base bias of Q_1. This results in reduction of conduction level of Q_1. Thus further increase in load current is prevented.

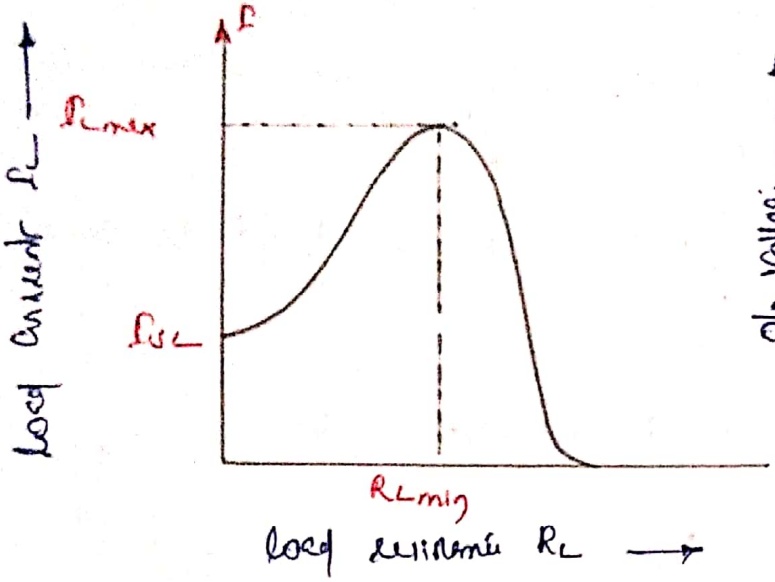
Due to reduction in load resistance V_{BE3} increases to a level at which Q_3 gets saturated. Now collector current I_{C3} becomes constant. Any further decrease in R_L will have no effect on I_{C3}. The corresponding load current I_{max} is

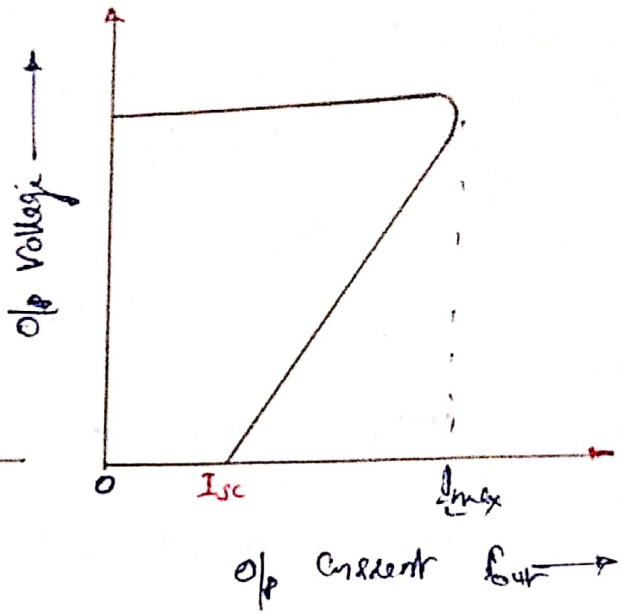
$$I_{max} = \frac{V_{BE3}}{k R_5} + \frac{(k-1)V_{out}}{k R_5}$$

Beyond this point V_{BE_3} drops due to saturation with load resistance $R_L = 0$ $V_{out} = 0$.

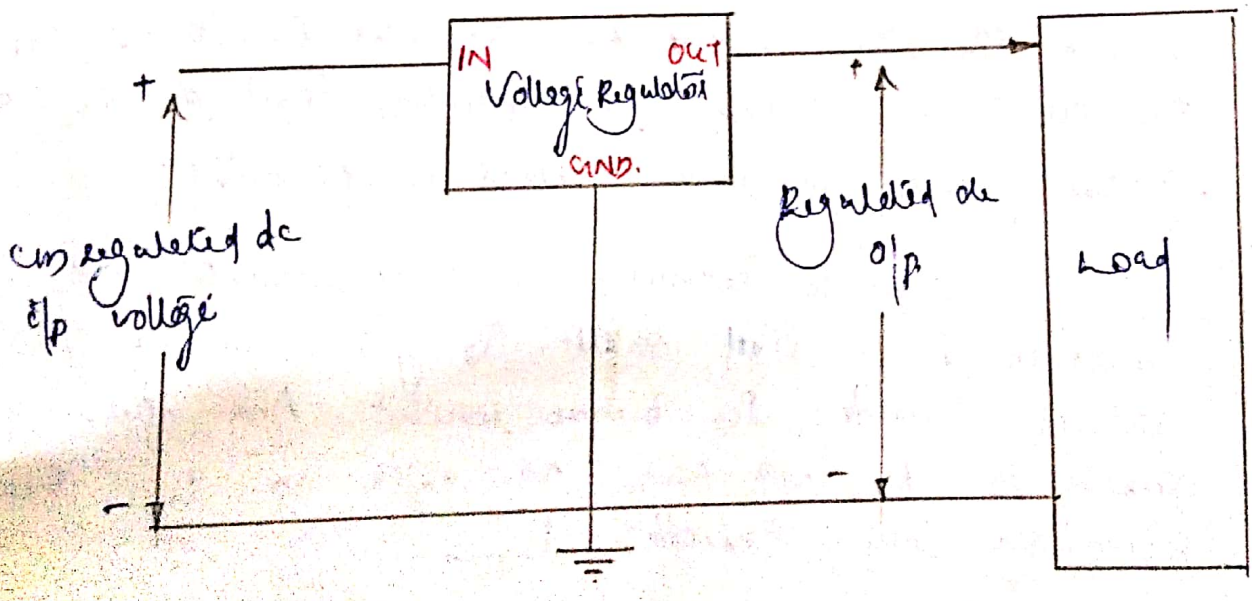
$$\therefore I_{SC} = \frac{V_{BE_3}}{R R_5}$$

Should load current I_{SC} is much less than $I_{L\,max}$ providing -fold back current limiting.





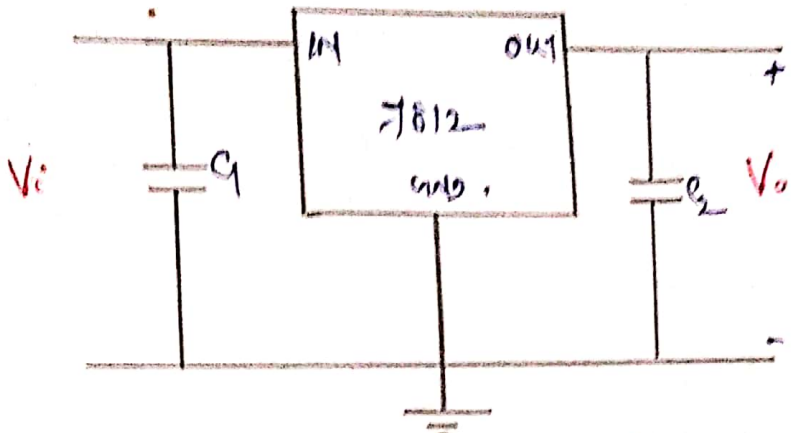
: Three Terminal Voltage Regulator:



Block representation of 3-Terminal voltage regulator.

Fixed voltage regulator has an unregulated dc i/p voltage applied to one i/p terminal, regulated o/p V_o from 3rd terminal and 2nd terminal connected to ground.

Fixed +ve Voltage Regulators: [78xx Series] (15)



Series 78 regulators provide fixed regulated voltages from 5V to 24V. In 78XX unregulated i/p Vi is ~~applied~~ filtered by capacitor C and connected to IC's IN terminal. IC's out terminal provides regulated +12V. 3rd terminal is connected to ground.

IC part	O/p Voltage V_o
7805	+5
7806	+6
7808	+8
7810	+10
7812	+12
7815	+15
7818	+18
7824	+24

+ve Voltage Regulators in 78xx Series.

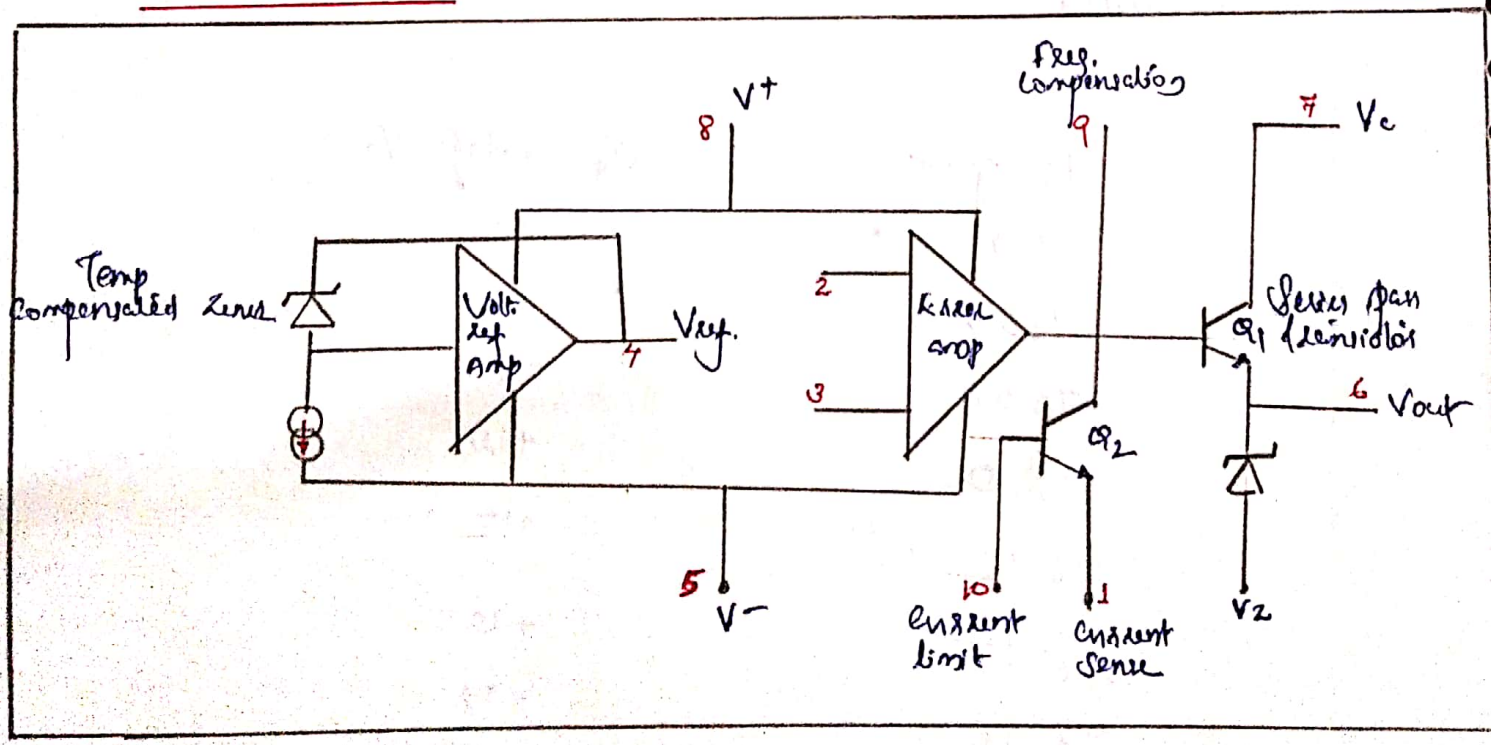
Fixed -ve Voltage Regulators: [79xx Series]

The Series 79xx provides -ve Voltages (regulated). It also provide regulated o/p from -5V to -24V.

Ic part	O/p voltage V
7905	-5
7906	-6
7908	-8
7909	-9
7912	-12
7915	-15
7918	-18
7924	-24

Adjustable Voltage Regulators:

Ic 723



Internal BD of 723

The internal working can be explained by dividing it into two blocks. Reference Voltage Generator and Error amplifier

In the reference voltage generator a Zener diode is being compelled to operate at a fixed point by a constant current source which comes along with an amplifier to generate a constant voltage of 7.15V at Vref pin of I.C.

Error amplifier section consisting of error amp. series pass transistor and a current limiting transistor. Error amp can be used to compare the o/p voltage applied at inverting input terminal and Vref applied at Non-inverting input terminal. Conduction of transistor Q_1 is controlled by error signal. & Q_1 controls o/p voltage.

16

: FIELD EFFECT TRANSISTORS:

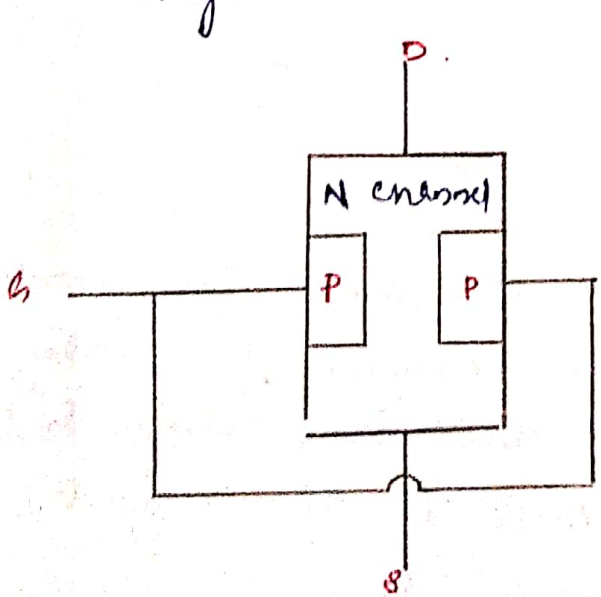
FET is a semiconductor device which depends for its operation on the control of current by an electric field.

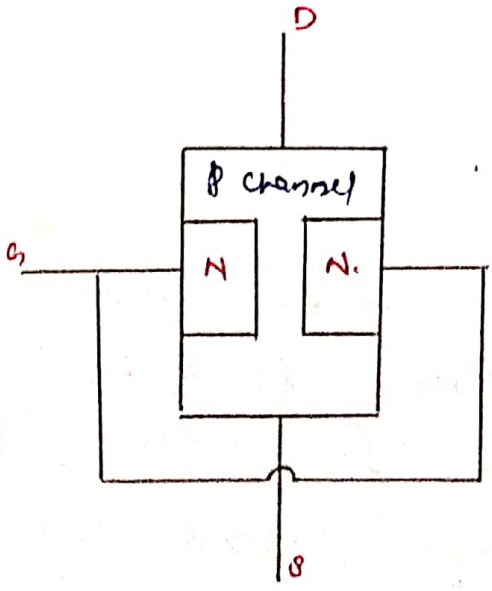
There are two types of FETs: (19)

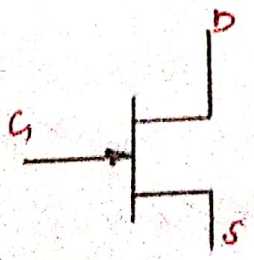
* JFET.
* MOSFETs [Insulated Gate FETs].

: Junction Field Effect Transistors:

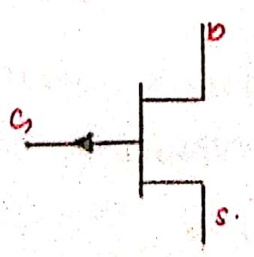
JFET are of two types N-channel and P-channel. In N-channel current conduction the 3 terminals of JFET are Gate, Source and Drain. Gate is controlling terminal. Source is the terminal through which charge carriers enter the device and drain is the terminal through which charge carriers leave the device.







N - channel

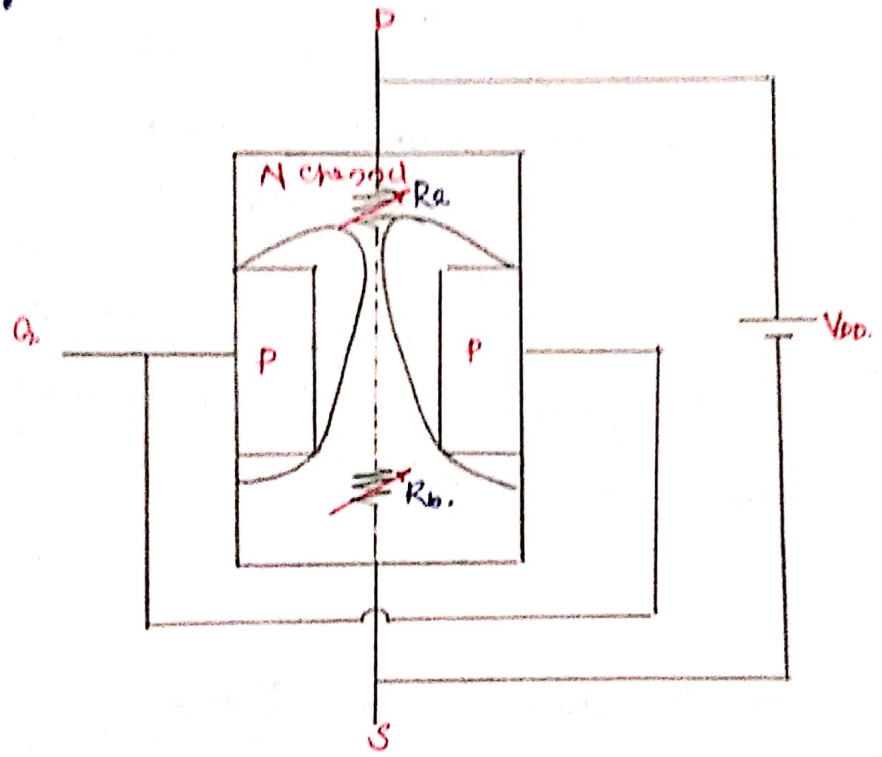


P- channel

Operation of JFET / Depletion layer formation in JFET

Here P type Gate & N type channel constitute a PN junction. This PN junction shown is reverse biased during JFET Operation. In a reverse biased junction there exist depletion region of immobile ions. This depletion region extends in N region where doping concentration is less.

The reverse bias can be obtained by applying voltage across Drain & Source.



In this channel we can assume two channel resistors Ra & Rb. The presence of supply VDD ensures Gate open, ē flow from Source to Drain through channel. and constitute the current known as Drain current ID.

This current causes voltage drop across channel resistance which has the effect of reverse biasing Gate to Source junction. even if Gate is open.

Here depletion region is not symmetrical because of the fact that reverse voltage is higher near the drain end compared to source end of channel.

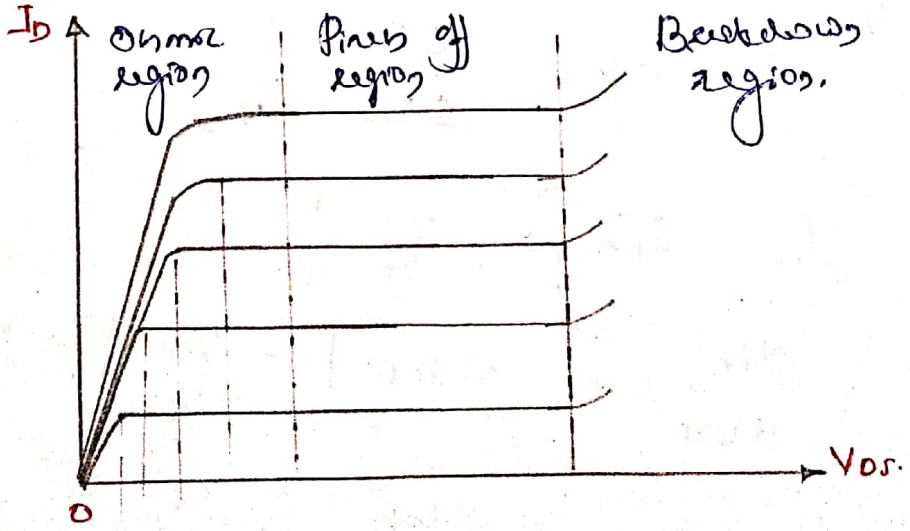
If V_{DS} is increased to a level where it appears that two depletion region would touch each other and is referred as Pinch off. The voltage at which this happens is called pinch off voltage V_p. At pinch off there exists saturation current I_{DSS}.

I_{DSS} is the maximum drain current for JFET and is defined by the condition $V_{GS} = 0$ & $V_{DS} > |V_p|$ The voltage V_{GS} can be used to control the drain current for JFET.

* JFET Characteristics *

VI Characteristics or Drain Characteristics:

It is the graph plotted between Drain current I_D and Drain to Source voltage V_{DS}. for different values of V_{GS}

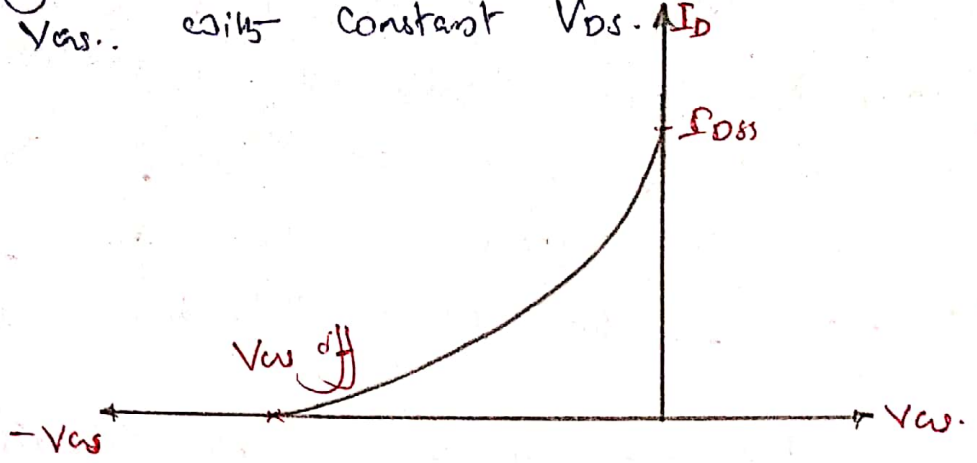


Current relation at Pinch off region

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2 \Rightarrow \text{Schockley's equation}$$

: Transfer Characteristics:

This is also called Transconductance Curve which gives relationship between Drain Current I_D and V_{GS}. with Constant V_{DS}.



: JFET Parameters:

1.) AC Drain ~~Current~~ resistance (R_d) = Dynamic drain resistance

$$R_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}}$$

2) Transconductance (g_m).

It is the ratio of change in drain current to change in gate to source voltage at constant V_{DS}

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}}$$

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$\frac{dI_D}{dV_{GS}} = 2 I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right] \cdot \frac{-1}{V_P}$$

$$\boxed{g_m = \frac{-2 I_{DSS}}{V_P}\left[1 - \frac{V_{GS}}{V_P}\right]}$$

When $V_{GS} = 0$ $\quad g_{m0} = -2 I_{DSS}/V_P$.

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right]$$

3) Amplification factor (μ)

It is the ratio of change in V_{DS} to change in V_{GS} at constant drain current.

$$\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D}$$

$$\mu = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\boxed{\mu = R_d \cdot g_m}$$

4) DC drain resistance R_D.

It is also called static or Ohmic resistance.

$$R_D = \frac{V_{DS}}{I_D}$$

(19)

Comparison between JFET & BJT.

JFET	BJT.
1. Unipolar device conduction occurs due to flow of either e^- or hole.	* Bipolar device conduction occurs due to both e^- & hole
2. Voltage controlled device Gate voltage controls drain current	* Current controlled device Base current controls collector current
3. High i/p impedance (MΩ)	* low i/p impedance (kΩ)
4. Negative temp coefficient	* Positive temp coefficient
5. Higher Switching Speed	* Lower Switching Speed
6. Generate less noise	* Generate more noise
7. Occupies less space in IC	* Occupies more space in IC
8. power consumption is low	* High power consumption.

Metal Oxide Semiconductor FET. (MOSFET)

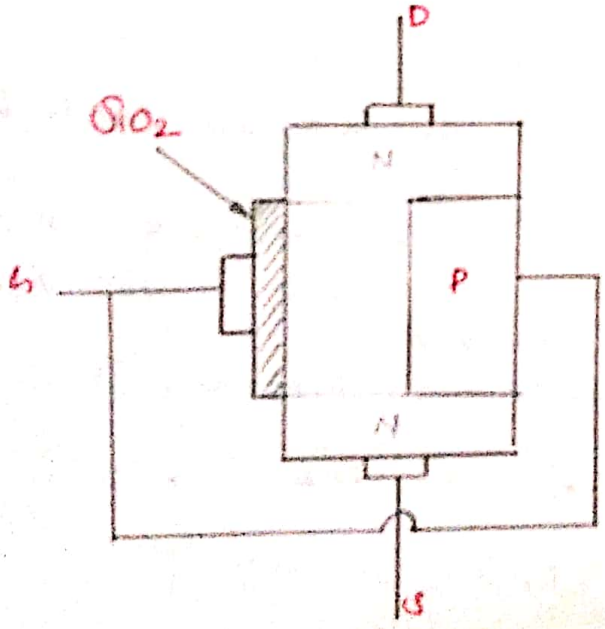
MOSFET is also called as Insulated Gate FET (IGFET). There is no direct electrical contact between gate & channel of MOSFET. Due to the presence of Insulator (SiO_2) between gate & channel MOSFET poses very high i/p impedance. and there is no gate current.

MOSFETs are of two types depending on whether the channel is already present or not,

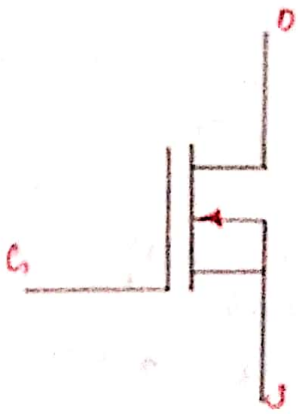
* Depletion type MOSFET
* Enhancement type MOSFET.

D-MOSFET

D type MOSFET is the one in which there exists an inherent channel.



N channel D MOSFET



Symbol.

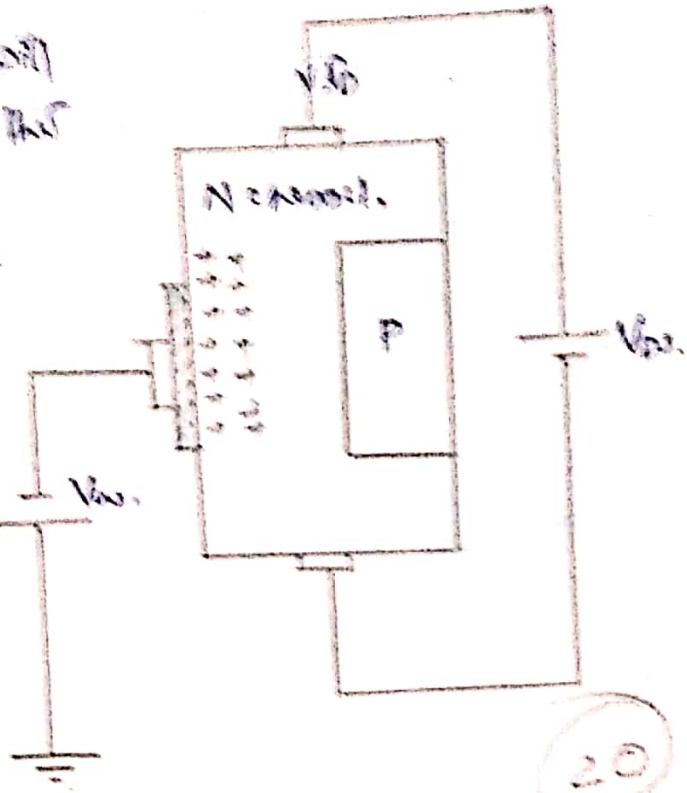
Operation

when $V_{GS}=0$ and V_{DS} is applied then Drain & Source. This results in attraction of $\bar{e}$ in channel towards the potential of Drain terminal and drain

current is controlled through N channel.
This current Id with Vds is called Idss
as in JFET.

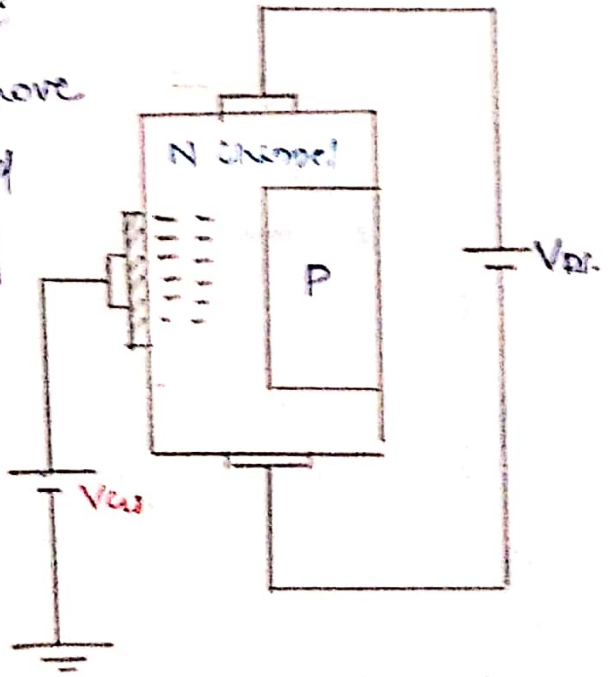
Depletion mode of Operation:

when V_{GS} is -ve, it will attract the holes towards the gate end of channel.
This tends to reduce the effective width of channel and this reduces the conductivity and therefore Drain current decreases.

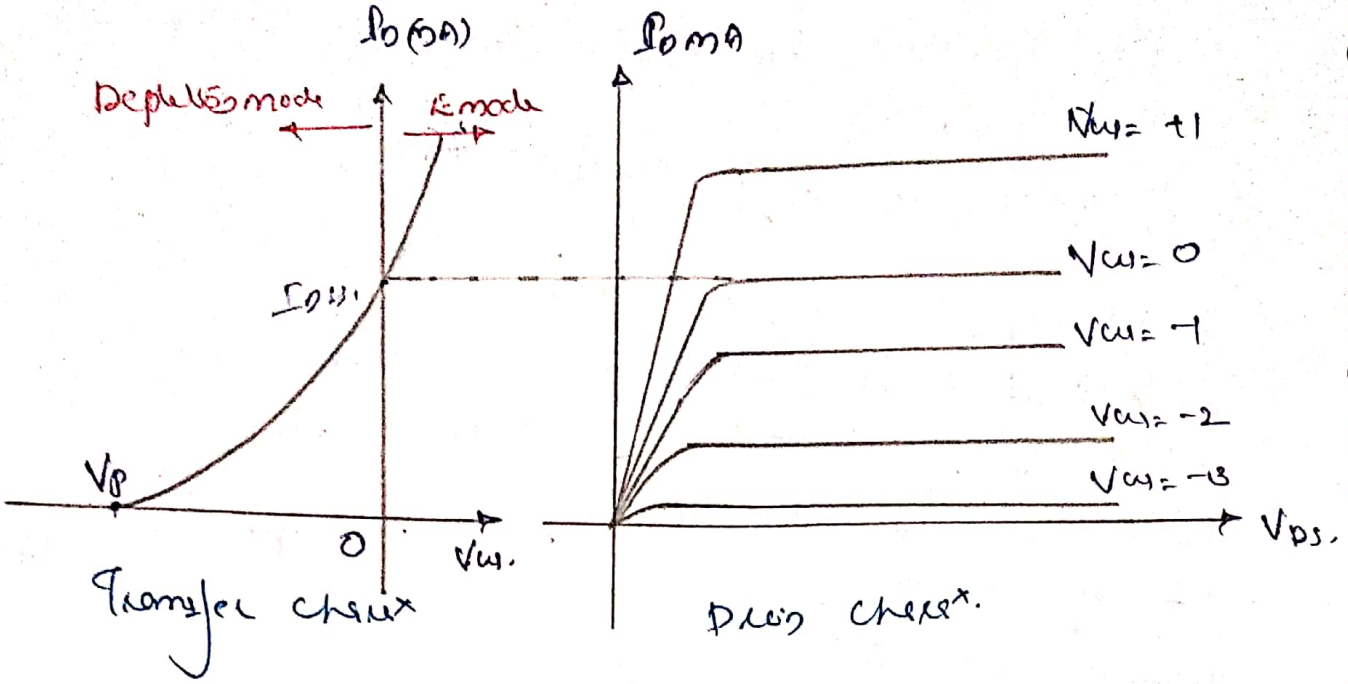


Enhancement mode of Operation:

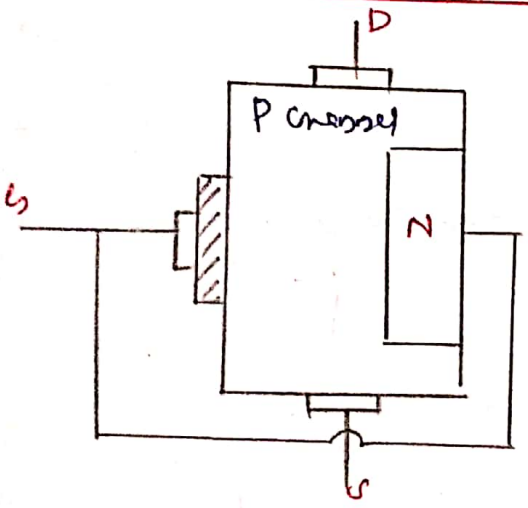
The positive gate voltage causes free electrons to move from substrate to channel and resulting in increased drain current.
This drain current increases with increase in V_{GS}. Hence channel is enhanced during the V_{GS}.



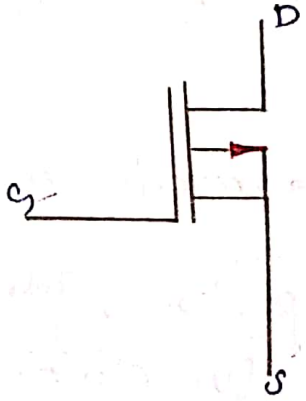
Current equation Id: R[



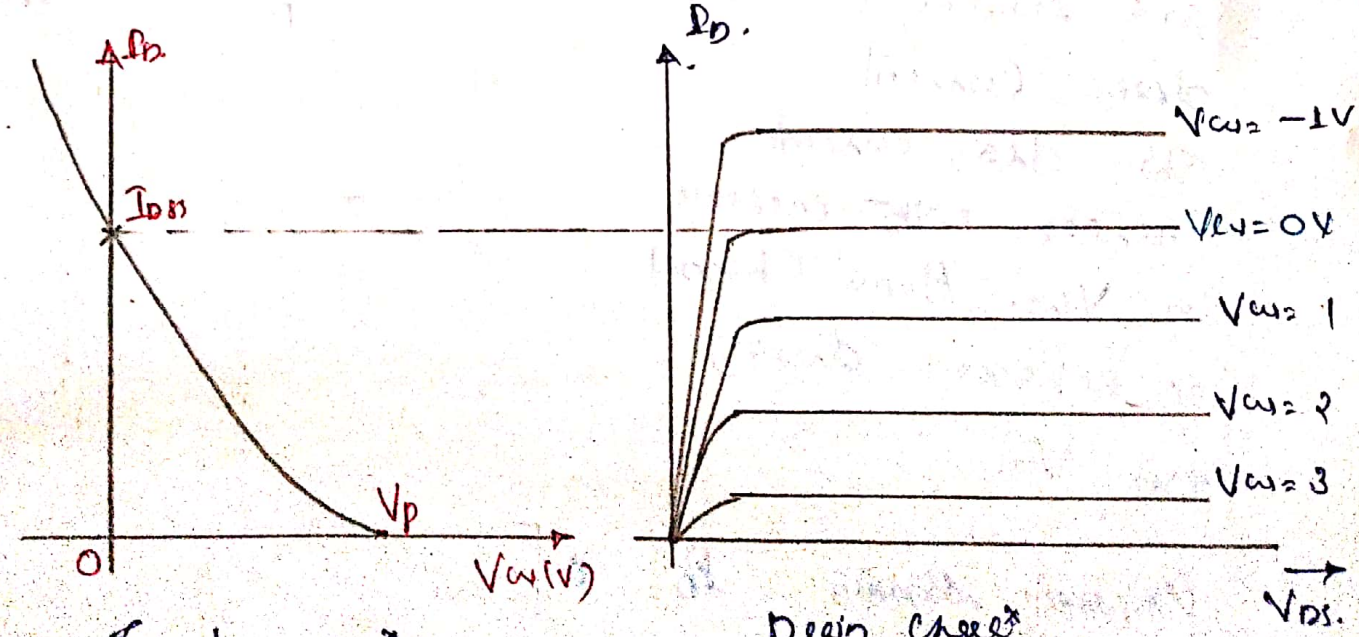
P- Channel D- MOSFET.



Structure

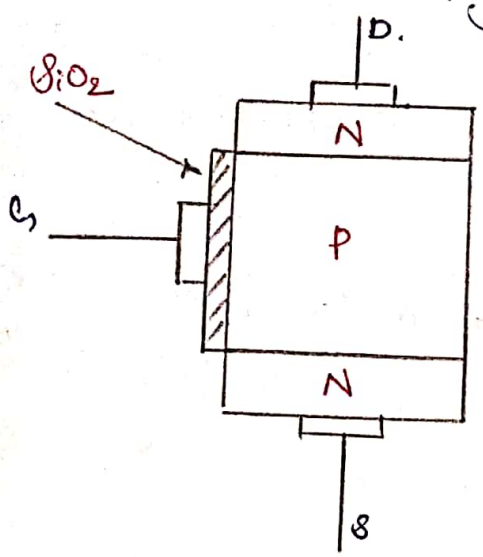


Symbol.

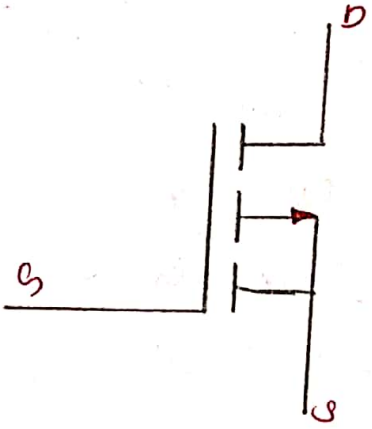


Enhancement Type MOSFET.

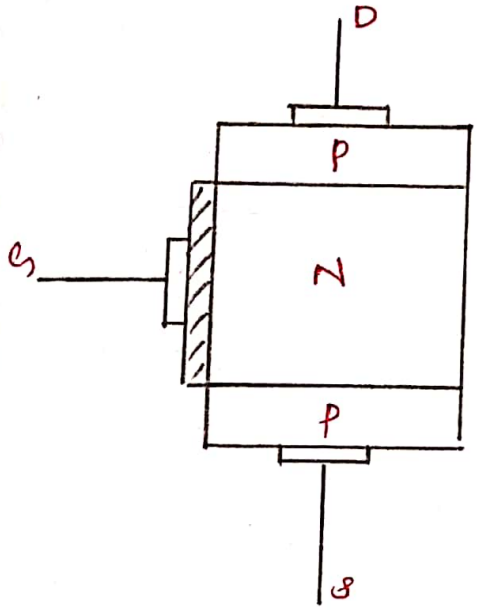
In E-MOSFET, there is no inherent channel. It can work only in Enhancement mode.



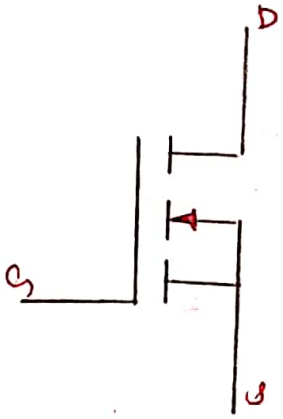
P Channel MOSFET



Symbol.



N Channel MOSFET

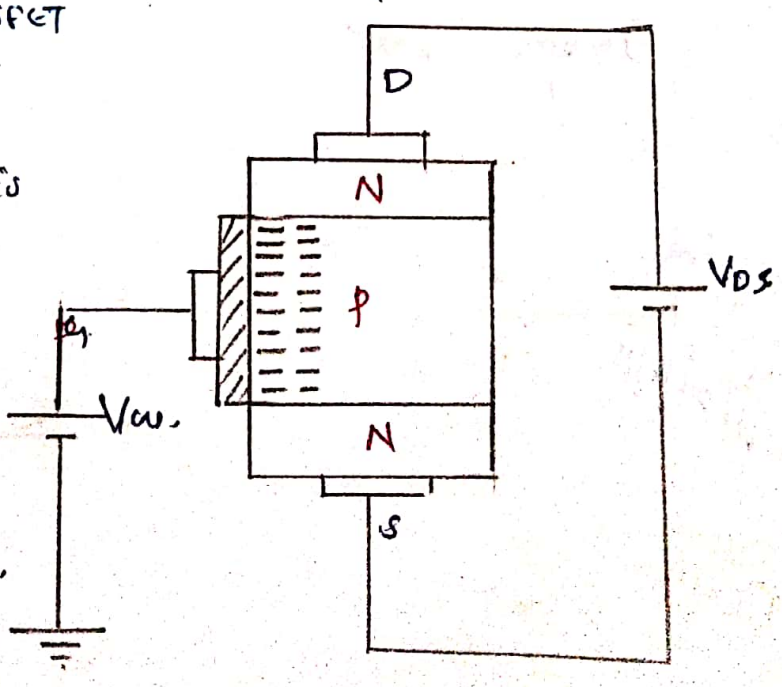


Symbol.

21

Operation

In E MOSFET there is no inherent Channel. By the application of +ve V_{GS}, it will attract e to the gate end of MOSFET.

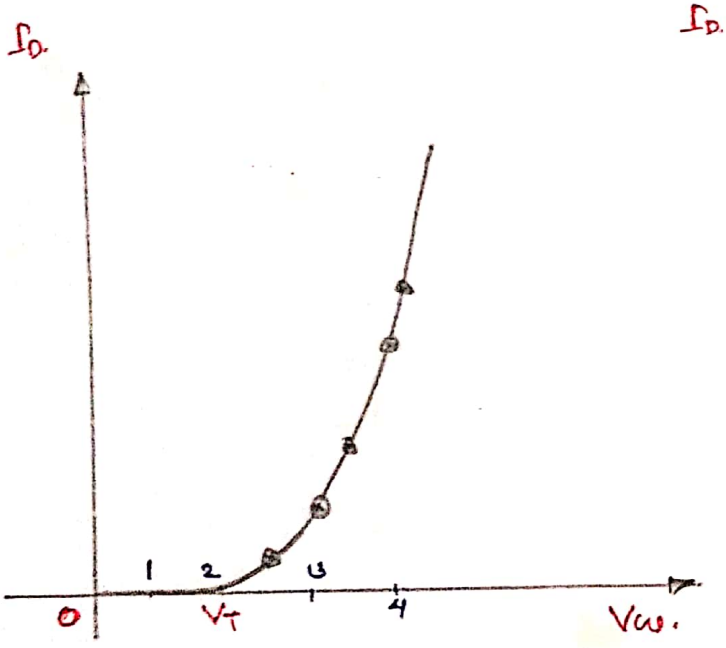


and thus by creates a layer of $\bar{e}$ which creates a channel b/w Drain & Source. ∴ Drain Current I_D flows through the device

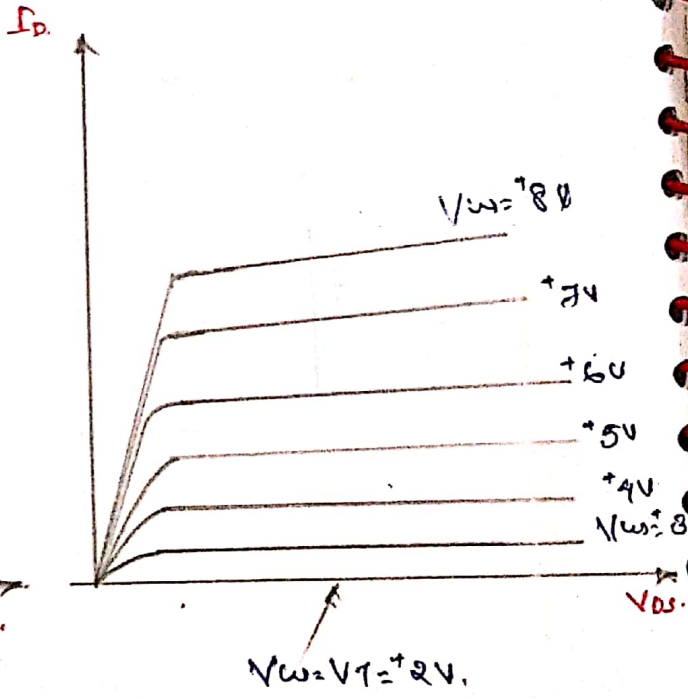
$$I_D = K[V_{GS} - V_{GS_{TH}}]^2$$

$V_{GS_{TH}}$ is the voltage at which channel is created b/w Drain & Source

The gate to Source voltage required to create a channel between Source & Drain and thus to turn ON the transistor is known as Threshold Voltage



Transfer Char^x



Drain Charax.

Verified
22/8/16
18/11/16